

# EA30\_BM

## Schematics Document

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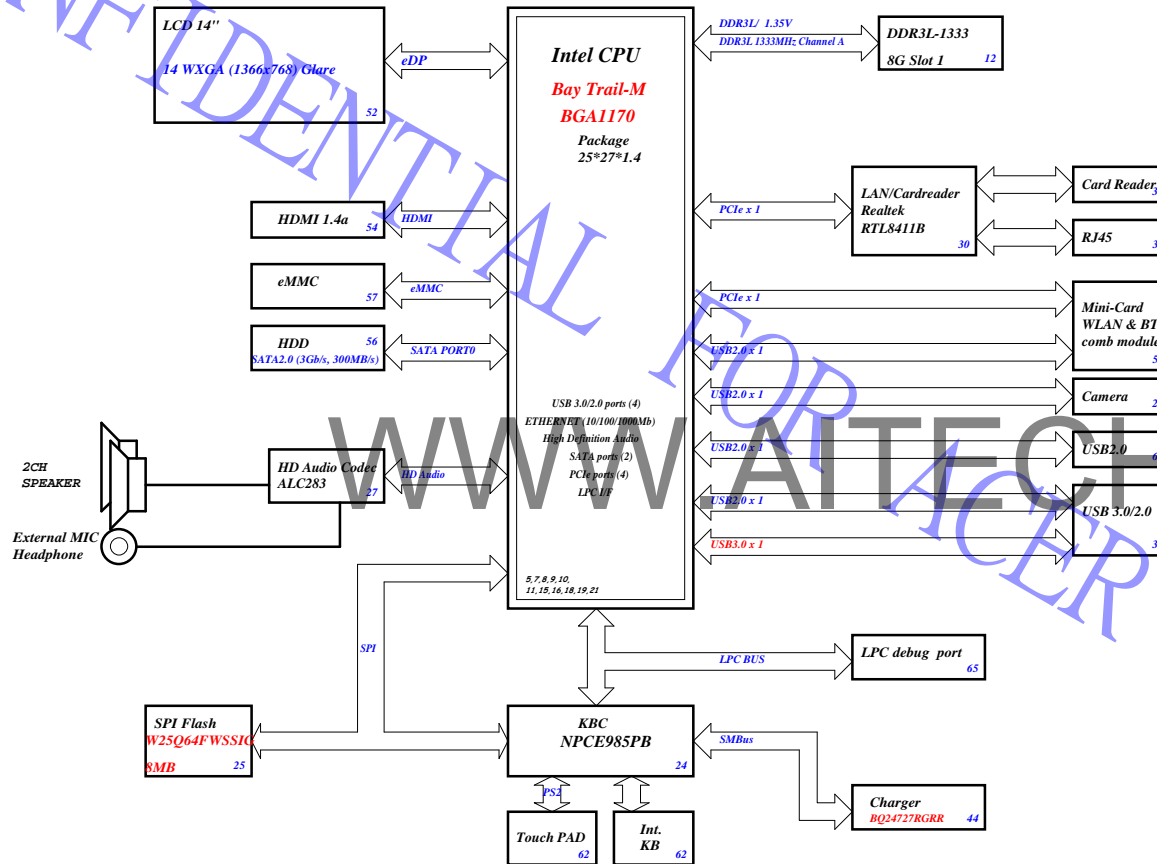
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Cover Page			
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# EA30\_BM Board Block Diagram

Project code :  
PCB P/N : 14221  
Revision : SB



CHARGER	
BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5
DCBATOUT	3D3V_S5
CPU DC/DC	
ISL95833	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SY8208	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
SYSTEM DC/DC	
SY8208DQNC	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM LDO	
TLV70218	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
TLV70012	51
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5
Step Down Regulator	
SYW232	51
INPUTS	OUTPUTS
1D0V_S0_PG	1D05V_S0
GPU Core	
RT8812	82
INPUTS	OUTPUTS
DCBATOUT	V6A_CORE
LOAD SWITCH	
TPS22966	37
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
LOAD SWITCH	
TPS22965	37
INPUTS	OUTPUTS
1D0V_S5	1D0V_S0
SYSTEM DC/DC	
SY8208	83
INPUTS	OUTPUTS
DCBATOUT	1D5V_V6A_S0
LOAD SWITCH	
TPS22966	83
INPUTS	OUTPUTS
1D05V_S0	1D5V_V6A_S1
3D3V_S0	3D3V_V6A_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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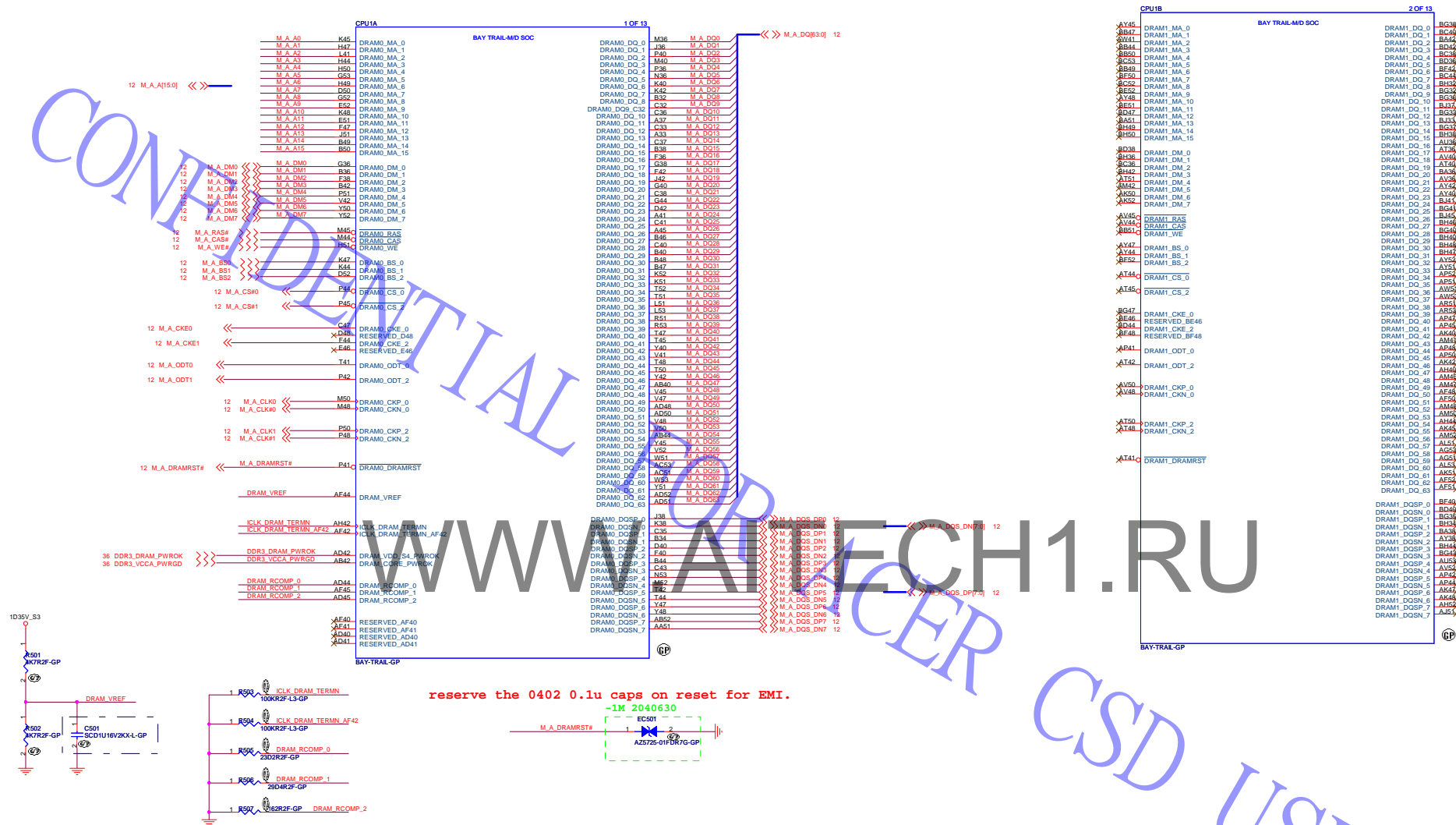
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Title **CPU (Reserved)**

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SSID = CPU

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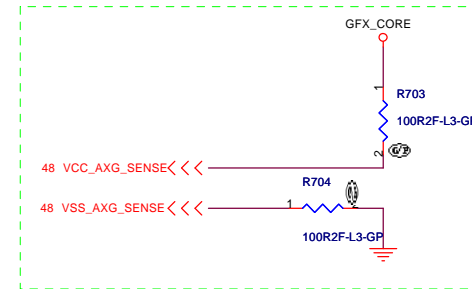
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**CPU (CFG)**

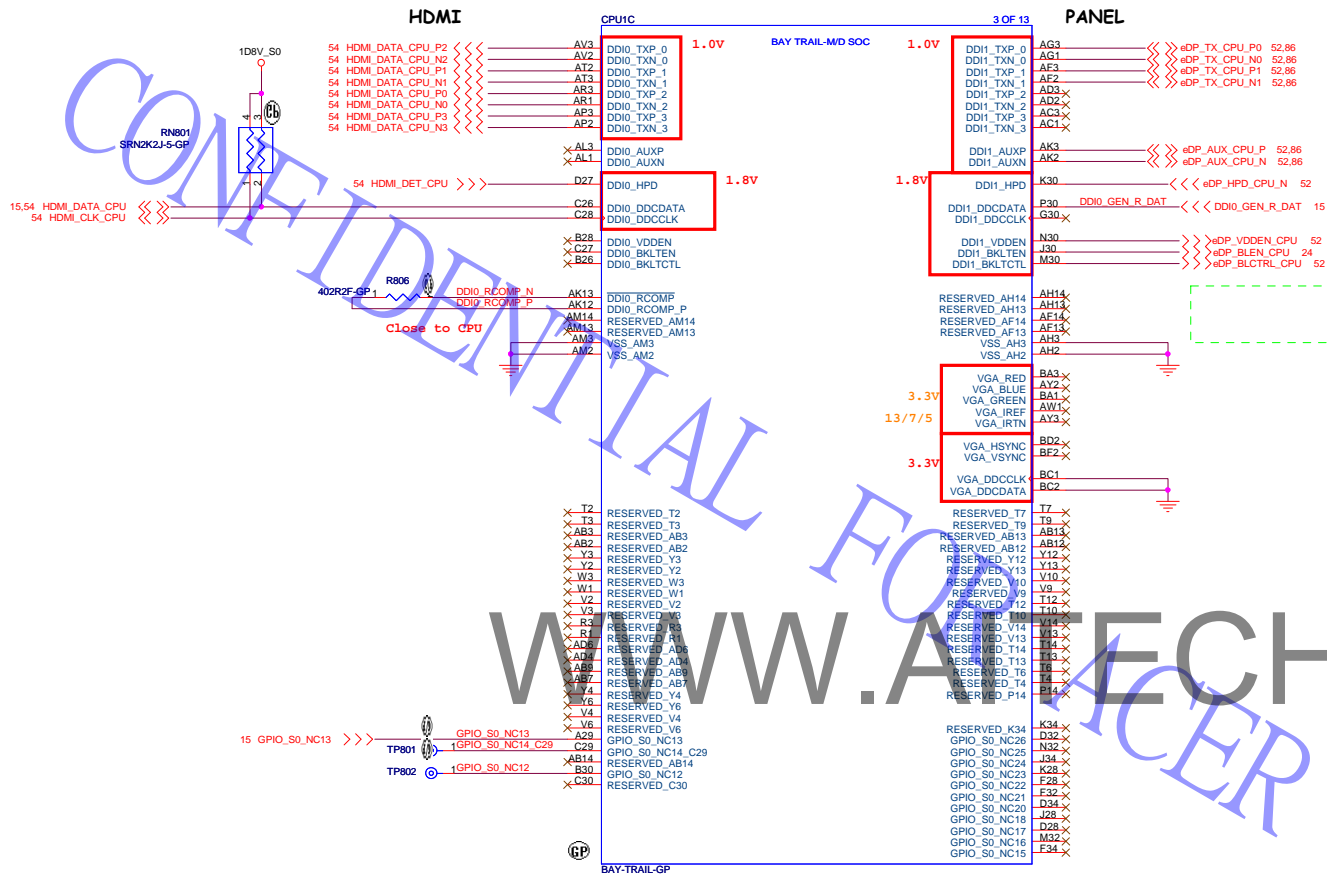
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SA 20140502-1



Title			
<b>CPU (VCC CORE)</b>			
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CPU (DDI/EDP/GPIO)			
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SSID = CPU

CPU1I 9 OF 13		
BAY TRAIL-M/D SOC		
A11	VSS1	VSS36
A15	VSS2	VSS37
A19	VSS3	VSS38
A23	VSS4	VSS39
A27	VSS5	VSS40
A31	VSS6	VSS41
A35	VSS7	VSS42
A39	VSS8	VSS43
A43	VSS9	VSS44
A47	VSS10	VSS45
AA1	VSS11	VSS46
AA16	VSS12	VSS47
AA19	VSS13	VSS48
AA21	VSS14	VSS49
AA3	VSS15	VSS50
AA32	VSS16	VSS51
AA35	VSS17	VSS52
AA38	VSS18	VSS53
AA53	VSS19	VSS54
AB10	VSS20	VSS55
AB4	VSS21	VSS56
AB41	VSS22	VSS57
AB45	VSS23	VSS58
AB47	VSS24	VSS59
AB48	VSS25	VSS60
AB50	VSS26	VSS61
AB51	VSS27	VSS62
AB6	VSS28	VSS63
AC16	VSS29	VSS64
AC18	VSS30	VSS65
AC19	VSS31	VSS66
AC21	VSS32	VSS67
AC25	VSS33	VSS68
AC33	VSS34	VSS69
AC35	VSS35	VSS70
BAY-TRAIL-GP		GP

CPU1J 10 OF 13		
BAY TRAIL-M/D SOC		
AG38	VSS71	VSS106
AH4	VSS72	VSS107
AH41	VSS73	VSS108
AH45	VSS74	VSS109
AH7	VSS75	VSS110
AH9	VSS76	VSS111
AJ1	VSS77	VSS112
AJ16	VSS78	VSS113
AJ21	VSS79	VSS114
AJ25	VSS80	VSS115
AJ27	VSS81	VSS116
AJ29	VSS82	VSS117
AJ3	VSS83	VSS118
AJ30	VSS84	VSS119
AJ32	VSS85	VSS120
AJ33	VSS86	VSS121
AJ35	VSS87	VSS122
AJ38	VSS88	VSS123
AJ53	VSS89	VSS124
AK10	VSS90	VSS125
AK14	VSS91	VSS126
AK16	VSS92	VSS127
AK33	VSS93	VSS128
AK41	VSS94	VSS129
AK44	VSS95	VSS130
AM12	VSS96	VSS131
AM19	VSS97	VSS132
AM24	VSS98	VSS133
AM25	VSS99	VSS134
AM29	VSS100	VSS135
AM33	VSS101	VSS136
AM35	VSS102	VSS137
AM36	VSS103	VSS138
AM40	VSS104	VSS139
M28	VSS105	VSS140
BAY-TRAIL-GP		GP

CPU1K 11 OF 13		
BAY TRAIL-M/D SOC		
AT24	VSS141	VSS176
AT27	VSS142	VSS177
AT30	VSS143	VSS178
AT35	VSS144	VSS179
AT38	VSS145	VSS180
AT4	VSS146	VSS181
AT47	VSS147	VSS182
AT52	VSS148	VSS183
AU1	VSS149	VSS184
AU24	VSS150	VSS185
AU3	VSS151	VSS186
AU30	VSS152	VSS187
AU38	VSS153	VSS188
AU51	VSS154	VSS189
AV12	VSS155	VSS190
AV13	VSS156	VSS191
AV14	VSS157	VSS192
AV18	VSS158	VSS193
AV19	VSS159	VSS194
AV24	VSS160	VSS195
AV27	VSS161	VSS196
AV30	VSS162	VSS197
AV35	VSS163	VSS198
AV38	VSS164	VSS199
AV47	VSS165	VSS200
AV51	VSS166	VSS201
AV7	VSS167	VSS202
AW13	VSS168	VSS203
AW19	VSS169	VSS204
AW27	VSS170	VSS205
AW3	VSS171	VSS206
AW35	VSS172	VSS207
AY10	VSS173	VSS208
AY22	VSS174	VSS209
AY32	VSS175	VSS210
BAY-TRAIL-GP		GP

CPU1L 12 OF 13		
BAY TRAIL-M/D SOC		
BF30	VSS211	VSS246
BF36	VSS212	VSS247
BF4	VSS213	VSS248
BG31	VSS214	VSS249
BG34	VSS215	VSS250
BG39	VSS216	VSS251
BG42	VSS217	VSS252
BG45	VSS218	VSS253
BG49	VSS219	VSS254
BJ11	VSS220	VSS255
BJ15	VSS221	VSS256
BJ19	VSS222	VSS257
BJ23	VSS223	VSS258
BJ27	VSS224	VSS259
BJ31	VSS225	VSS260
BJ35	VSS226	VSS261
BJ43	VSS227	VSS262
BJ47	VSS228	VSS263
BJ7	VSS229	VSS264
C14	VSS230	VSS265
C19	VSS231	VSS266
C31	VSS232	VSS267
C34	VSS233	VSS268
C42	VSS234	VSS269
C45	VSS235	VSS270
C49	VSS237	VSS272
D12	VSS238	VSS273
D16	VSS239	VSS274
D24	VSS240	VSS275
D30	VSS241	VSS276
D36	VSS242	VSS277
D38	VSS243	VSS278
E19	VSS244	VSS279
E35	VSS245	VSS280
BAY-TRAIL-GP		GP

CPU1M 13 OF 13		
BAY TRAIL-M/D SOC		
K9	VSS281	VSS316
L13	VSS282	VSS317
L19	VSS283	VSS318
L35	VSS284	VSS319
M19	VSS285	VSS320
M26	VSS286	VSS321
M27	VSS287	VSS322
M34	VSS288	VSS323
M35	VSS289	VSS324
M38	VSS290	VSS325
M47	VSS291	VSS326
M51	VSS292	VSS327
N1	VSS293	VSS328
N16	VSS294	VSS329
N38	VSS295	VSS330
N51	VSS296	VSS331
P13	VSS297	VSS332
P16	VSS298	VSS333
P19	VSS299	VSS334
P20	VSS300	VSS335
P24	VSS301	VSS336
P32	VSS302	VSS337
P35	VSS303	VSS338
P38	VSS304	VSS339
P4	VSS305	VSS340
P47	VSS306	VSS341
P52	VSS307	VSS342
P9	VSS308	VSS343
T40	VSS309	VSS344
U1	VSS310	VSS345
U11	VSS311	VSS346
U12	VSS312	VSS347
U14	VSS313	VSS348
U21	VSS314	VSS349
VSS315	VSS350	VSS350
BAY-TRAIL-GP		GP

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CPU (VSS)		
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CPU\_CORE

CPU\_CORE

SA 20140225 change to 0805

C1027

C1023

C1025

C1009

C1010

C1011

C1024

C1012

C1013

SC22U6D3V5MX-L3-GP

SC22U6D3V5MX-L3-GP

SC22U6D3V5MX-L3-GP

SC22U6D3V3MX-1-GP

SC22U6D3V3MX-1-GP

SC22U6D3V3MX-1-GP

SC22U6D3V5MX-L3-GP

SC22U6D3V3MX-1-GP

SC22U6D3V5MX-L3-GP

SA 20140416 change to 0603

Cap Modify  
(For power)

SA 20140225 P7 del close gap

1D35V\_S3

-1M 2040630

SA 20140225 P7 del close gap

1D35V\_S3

C1001

C1002

C1003

C1004

C1005

C1006

C1007

C1008

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

Do Not Stuff

Do Not Stuff

Do Not Stuff

Do Not Stuff

C1014

C1015

SC401U16V2KX-L-GP

SC401U16V2KX-L-GP

Close pin AD38 &amp; AF38

Cap Modify

Cap Modify

GFX\_CORE

GFX\_CORE

SA 20140225 change to 0603

C1016

C1017

C1018

C1019

C1020

C1021

SC22U6D3V3MX-1-GP

SC407U6D3V3KX-L-GP

SC407U6D3V3KX-L-GP

SC22U6D3V3MX-1-GP

SC22U6D3V3MX-1-GP

SC22U6D3V5MX-L3-GP

Cap Modify  
(For power)Cap Modify  
(For power)

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Title

CPU (Power CAP1)

Size  
A4

Document Number

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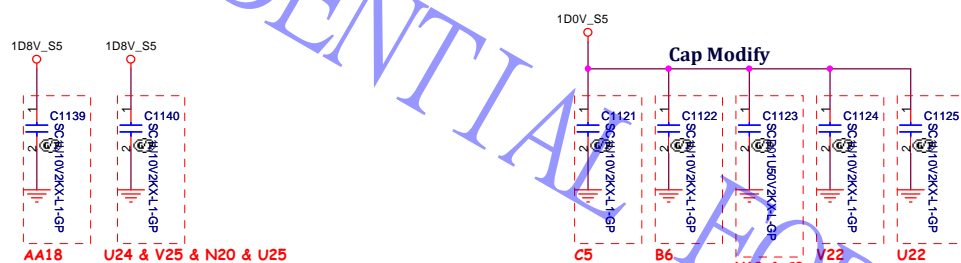
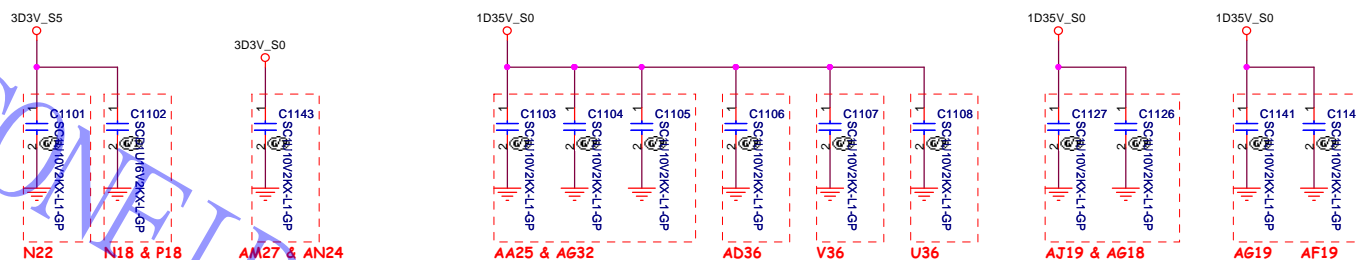
Rev  
-1

Date: Tuesday, July 08, 2014

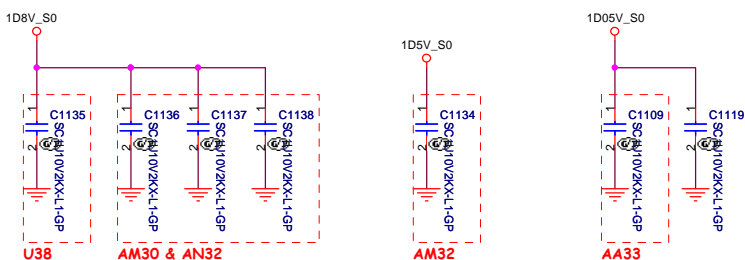
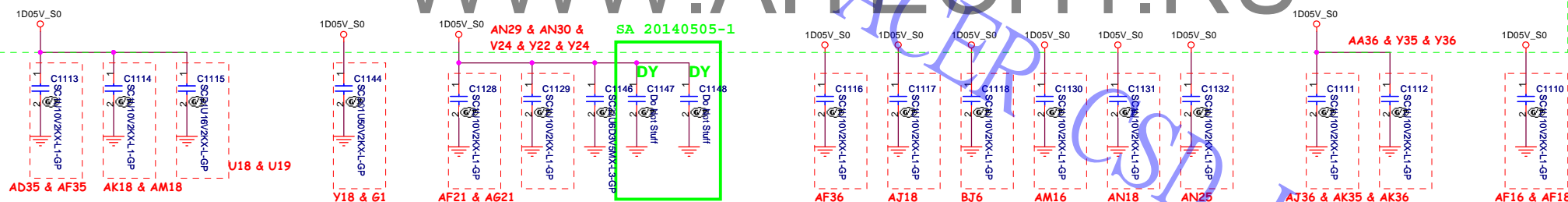
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## Cap Modify



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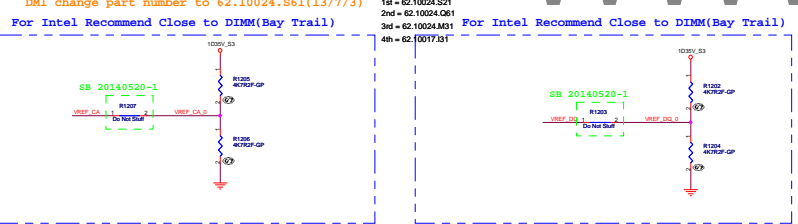
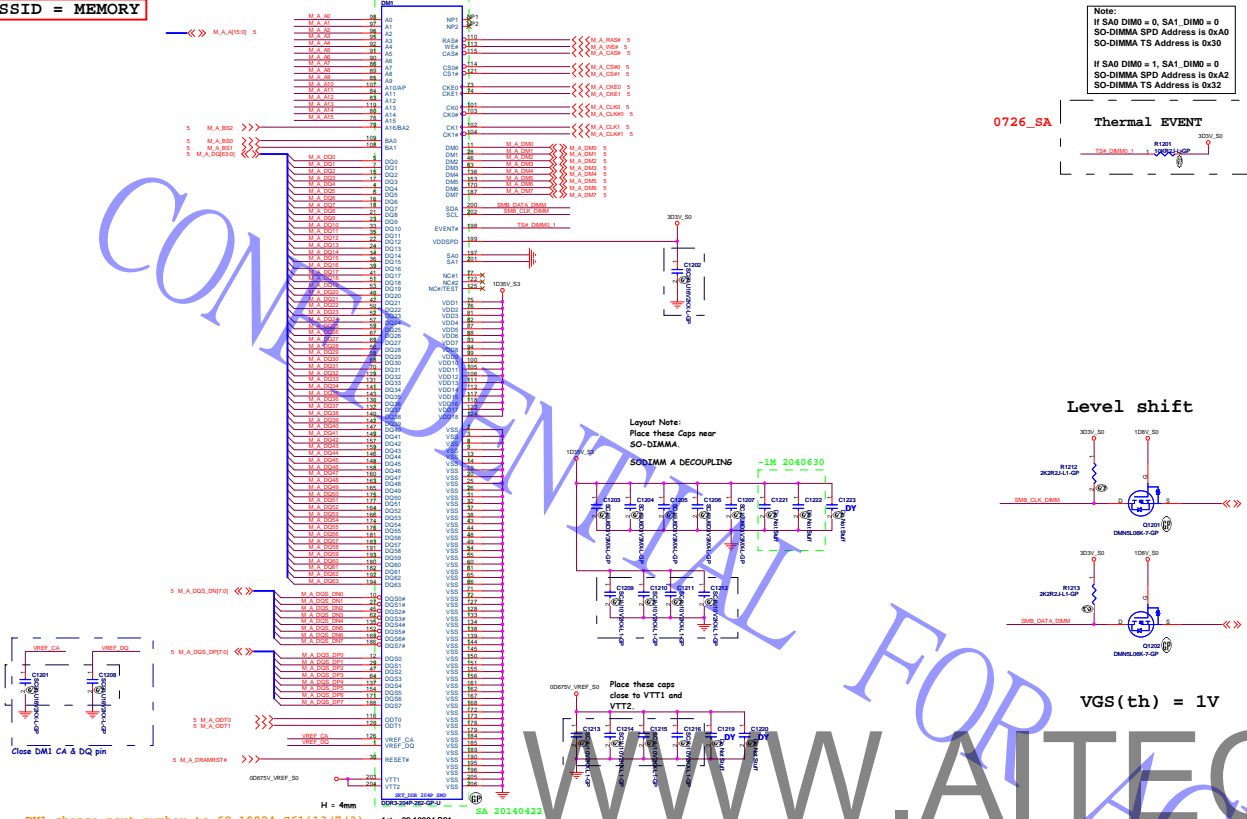


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Title			
<b>CPU (Power CAP2)</b>			
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SSID = MEMORY



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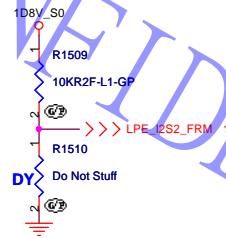
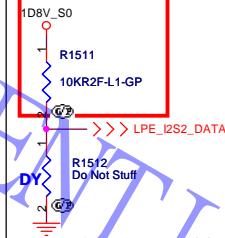
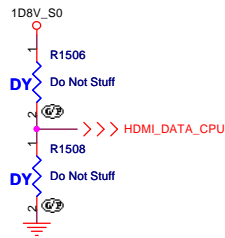
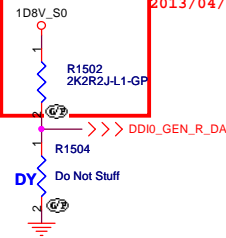
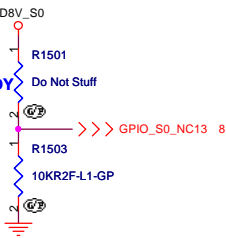
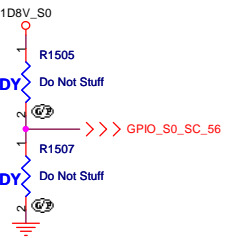
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**SSID = STRAP**

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI1 Detect	DDI0 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI1_DDCDATA	DDI0_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	RN801 PH DDI1 detected	DDI0 detected	DDI1 detected	
Low	LPC	Override	DDI1 not detected	DDI0 not detected	DDI1 not detected	

## 2.25 Hardware Straps

All straps are sampled on the rising edge of PMC\_CORE\_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

## 30.2 LPE\_I2S2\_DATAOUT / GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

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SSID = PCH

USB Table

Pair	Device
0	USB3.0 Port 0(USB2.0)
1	USB 2.0 (debug port)
2	WiFi + BT
3	Camera

USB 3.0

USB 2.0

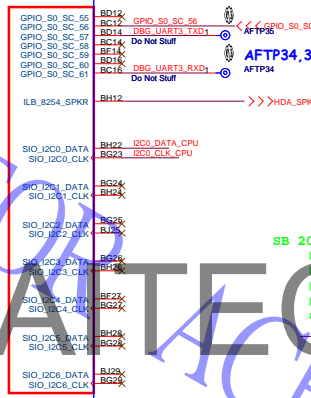
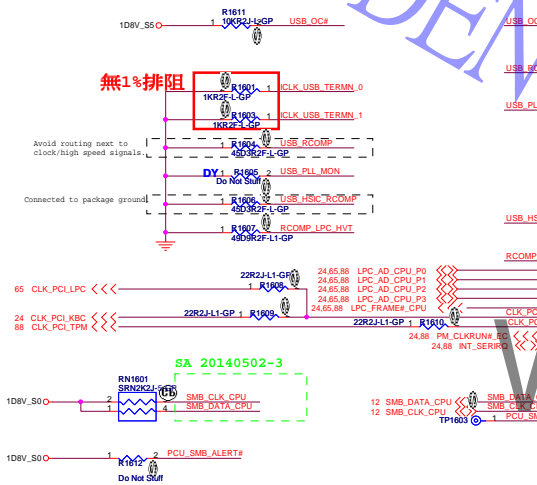
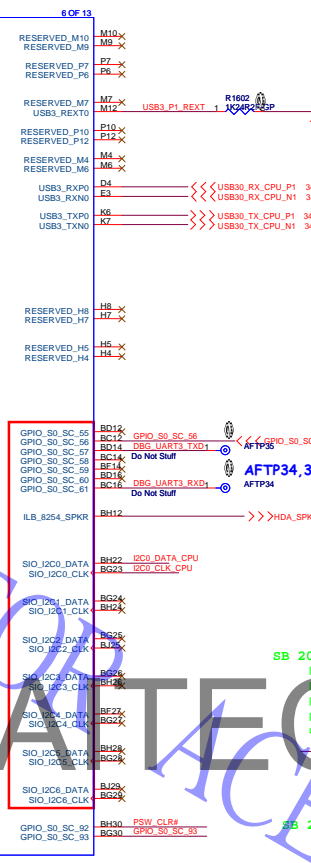
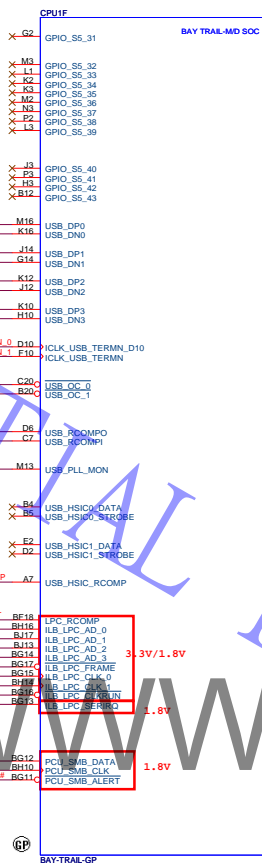
Wifi + BT

Camera

34 USB_CPU_PP0	>>>	USB_DP0
34 USB_CPU_PP0	>>>	USB_DN0
34 USB_CPU_PP1	>>>	USB_DP1
34 USB_CPU_PP1	>>>	USB_DN1
58,86 USB_CPU_PP2	>>>	USB_DP2
58,86 USB_CPU_PP2	>>>	USB_DN2
52,86 USB_CPU_PP3	>>>	USB_DP3
52,86 USB_CPU_PP3	>>>	USB_DN3

Close to CPU

13/7/5

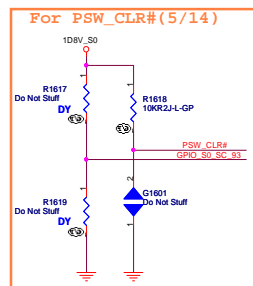


### USB Port Routing Guide for Bay Trail-M

WO/ Lighting Bolt(Can support 3 USB I/O Ports)

USB2/3 Camera Touch USB Hub

USB2 USB2 BT



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**CPU (DMI/FDI/PM)**

Size  
A4

Document Number

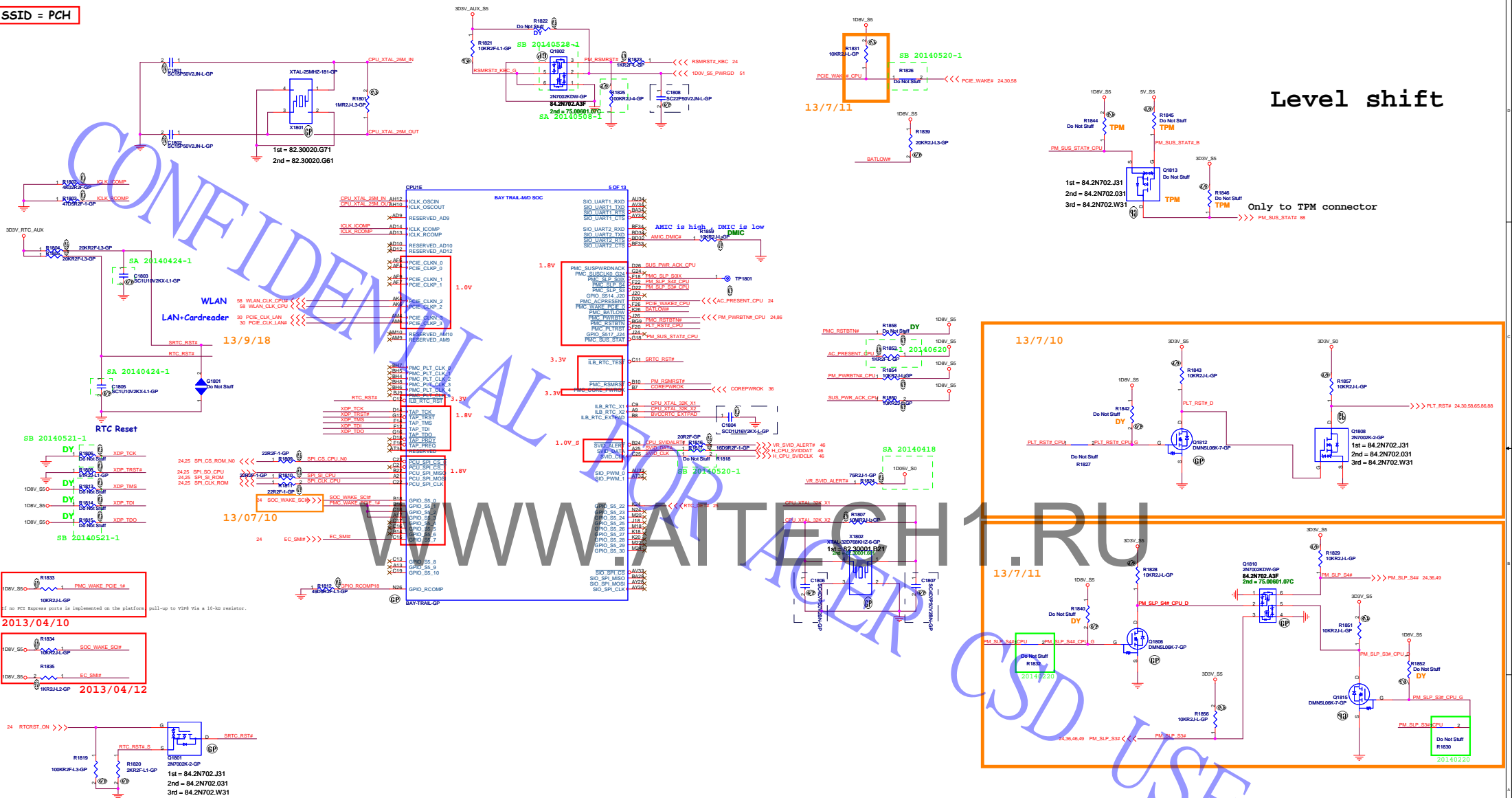
**EA30 BM**

Rev  
**-1**

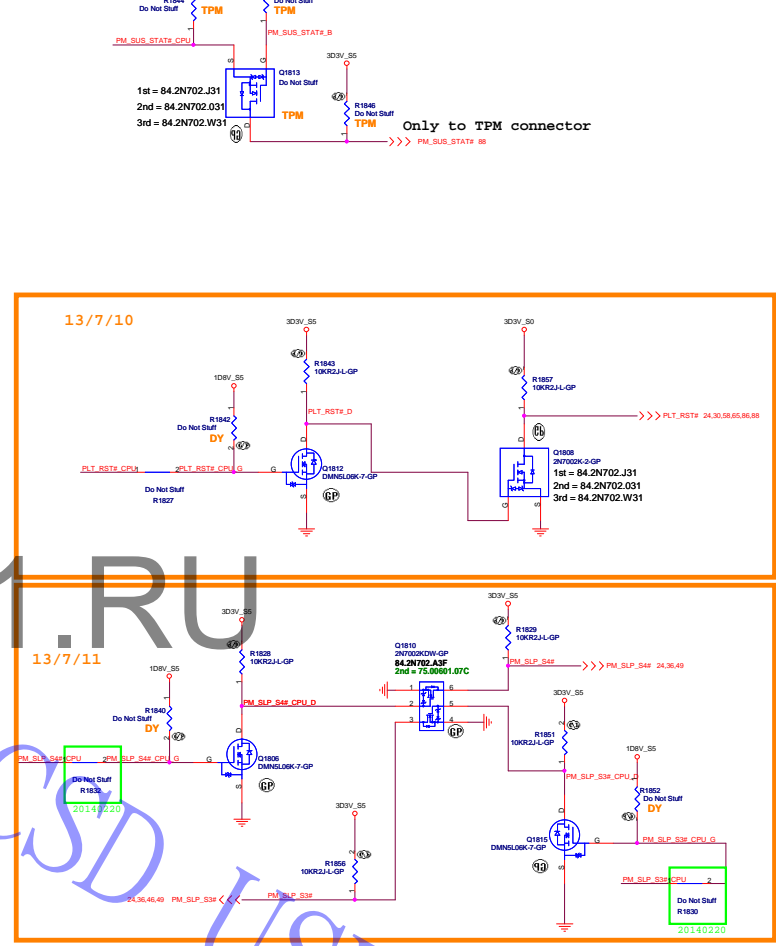
Date: Tuesday, July 08, 2014

Sheet 17 of 102

SSID = PCH



# Level shift

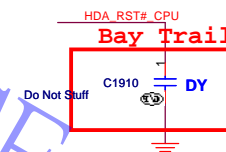
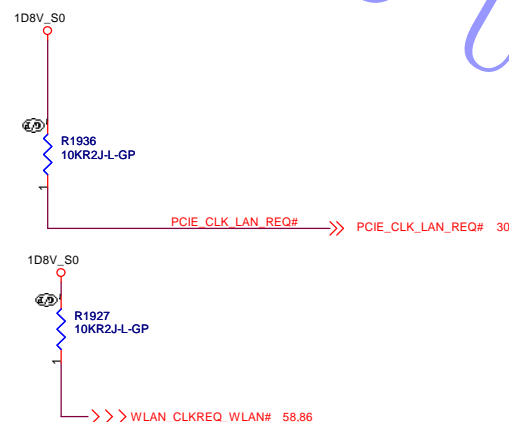
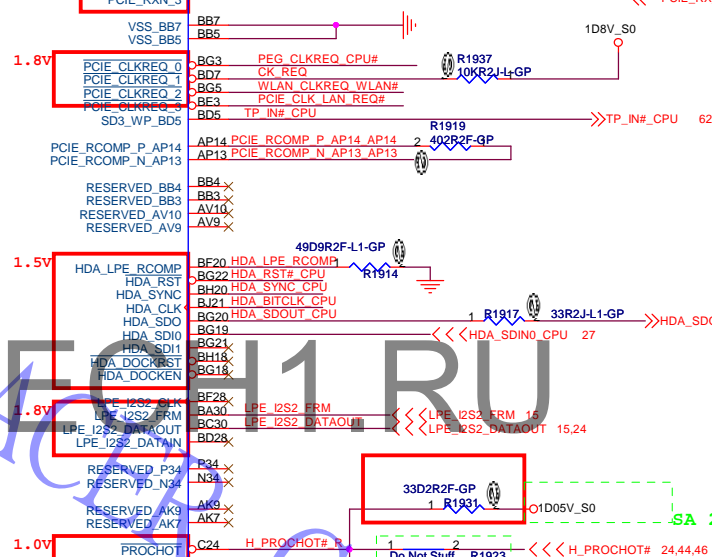
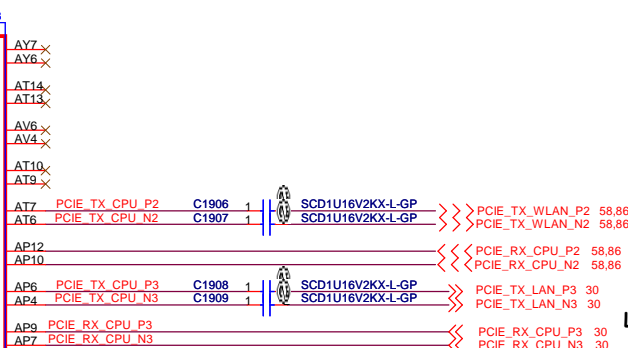
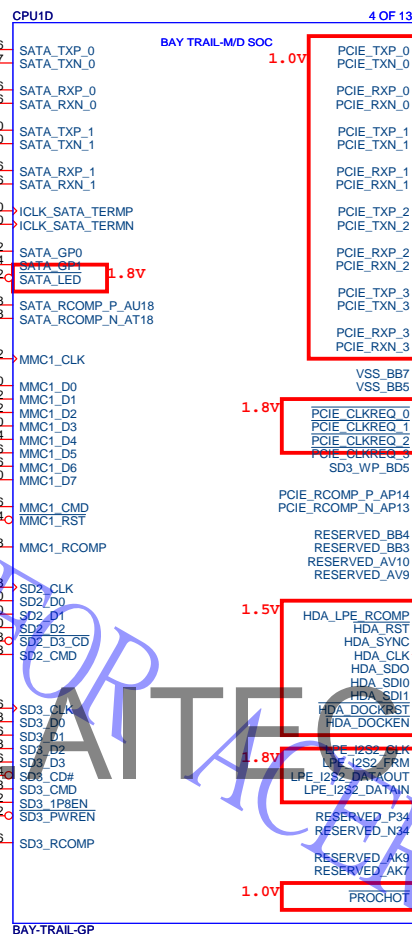
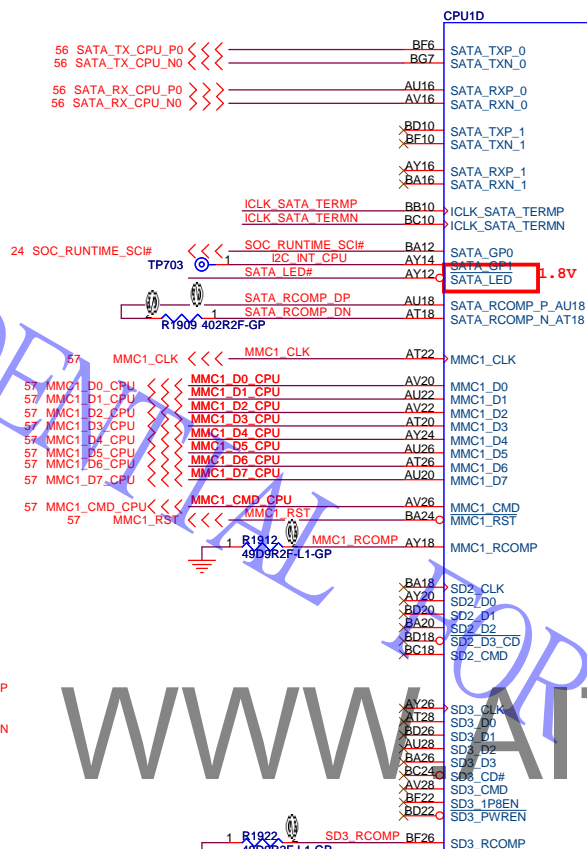
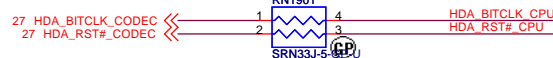
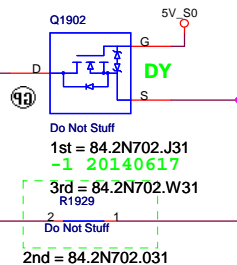
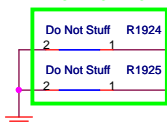
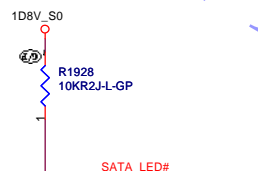


2013/04/10  
2013/04/12

**SSID = PCH**

HDD

ODD



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Title			
<b>CPU (SATA/PCIE/IHDA)</b>			
Size A3	Document Number		Rev
	<b>EA30_BM</b>		<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 19 of	102

SSID = PCH

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Title

**Reserved**

Size  
A4

Document Number

**EA30 BM**

Rev  
**-1**

Date: Tuesday, July 08, 2014

Sheet 20 of 102





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Title			
<b>Reserved</b>			
Size Custom	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
Date: Tuesday, July 08, 2014		Sheet 22 of	102

SSID = PCH

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Title

**CPU (VSS)**

Size  
Custom

Document Number

**EA30 BM**

Rev

**-1**

Date: Tuesday, July 08, 2014

Sheet 23 of 102

SSID = KBC

SB 20140520-1

Level shift

2013/05/21

13/7/14

WWW.ATCACER.CSD

PCB_VER_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	>= 2.618 V
SC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V
-1	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	#VALUE!
ADT_TYPE_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V	3.3000	>= 3.000 V
90W	100.0 K	N/A	0.000 V	0.0000	< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	>= 0.150 V
40W	20.0 K	100.0 K	0.550 V	0.5592	>= 0.425 V
MODEL_ID_AD	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
EA30_FANLESS	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
EA30_FAN	100.0 K	20.0 K	2.750 V	2.7591	>= 2.618 V
EA53_FANLESS	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V
EA53_FAN	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V
EA30_FANLESS_EMMC	100.0 K	64.9 K	2.000 V	2.0054	>= 1.875 V
EA30_FAN_EMMC	100.0 K	76.8 K	1.750 V	1.7591	>= 1.625 V
Reserved for project use	100.0 K	100.0 K	0.000 V	0.0000	< 1.758 V

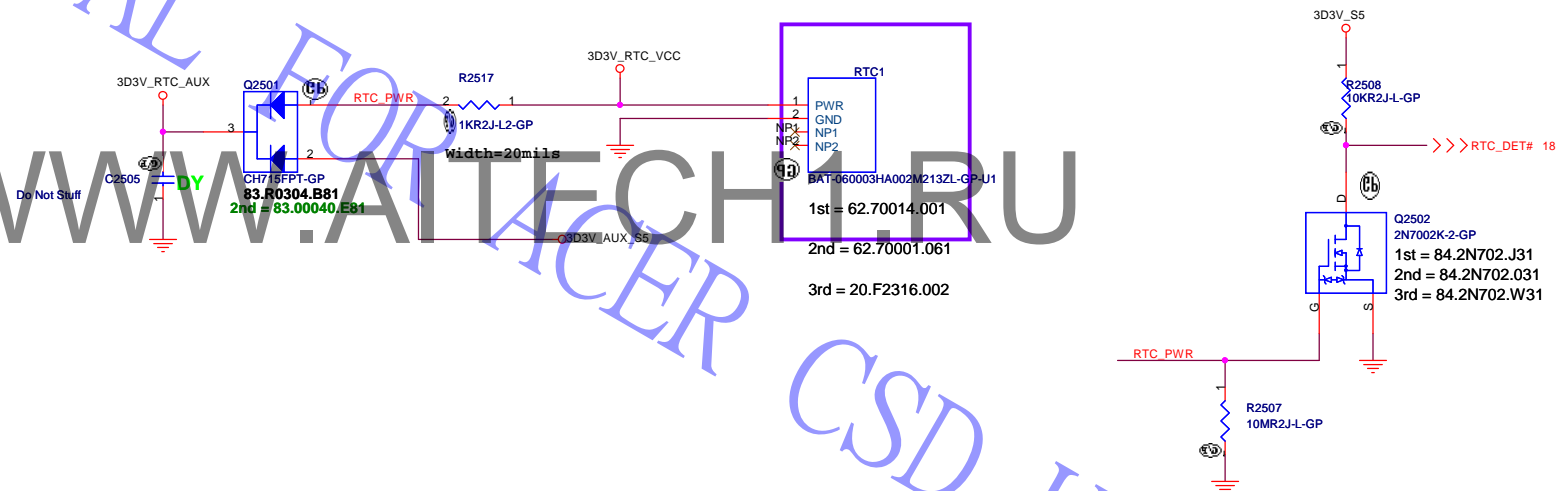
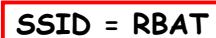
緯創資通 Wistron Corporation

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Model Number EA30 BM

Date: Tuesday, July 08, 2014

**SPI FLASH ROM (8M byte) for PCH**



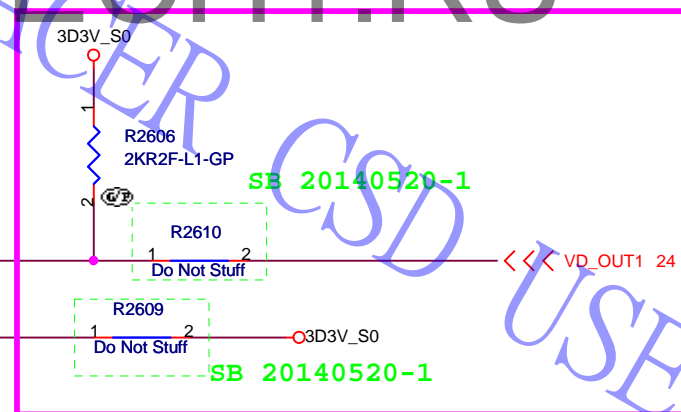
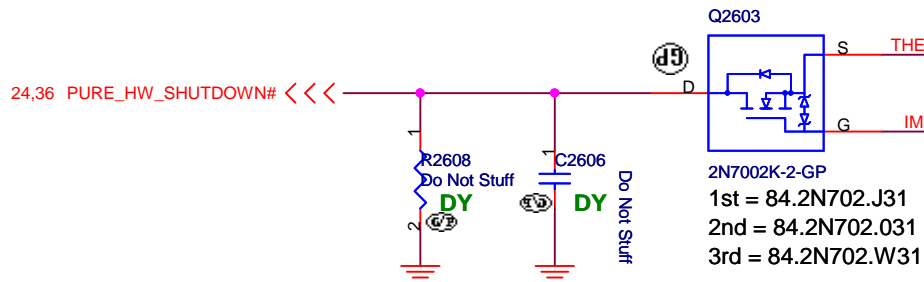
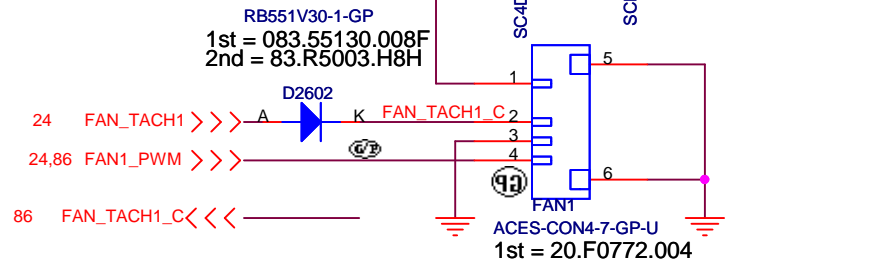
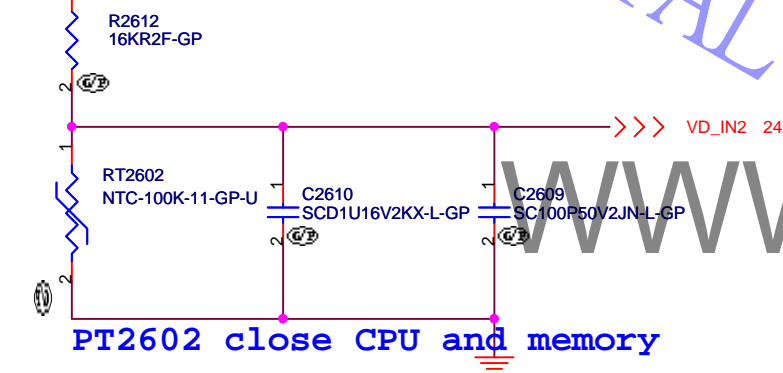
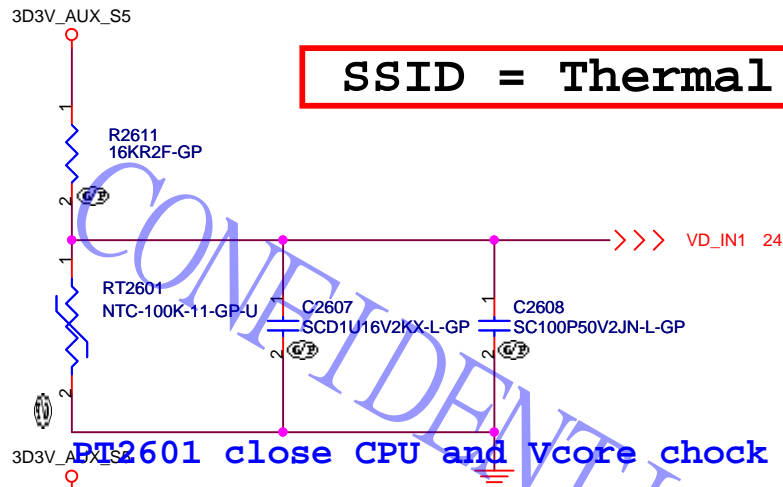
*SPI ROM Equal length need to less than 500mil*

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Title			
<b>Flash(KBC+PCH)/RTC</b>			
Size A3	Document Number		Rev
	<b>EA30 BM</b>		<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 25 of	102

SSID = Thermal



No eMMC

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

G788P81/Fan Controller P2793

Size  
A4

Document Number

EA30 BM

Rev  
-1

Date: Tuesday, July 08, 2014

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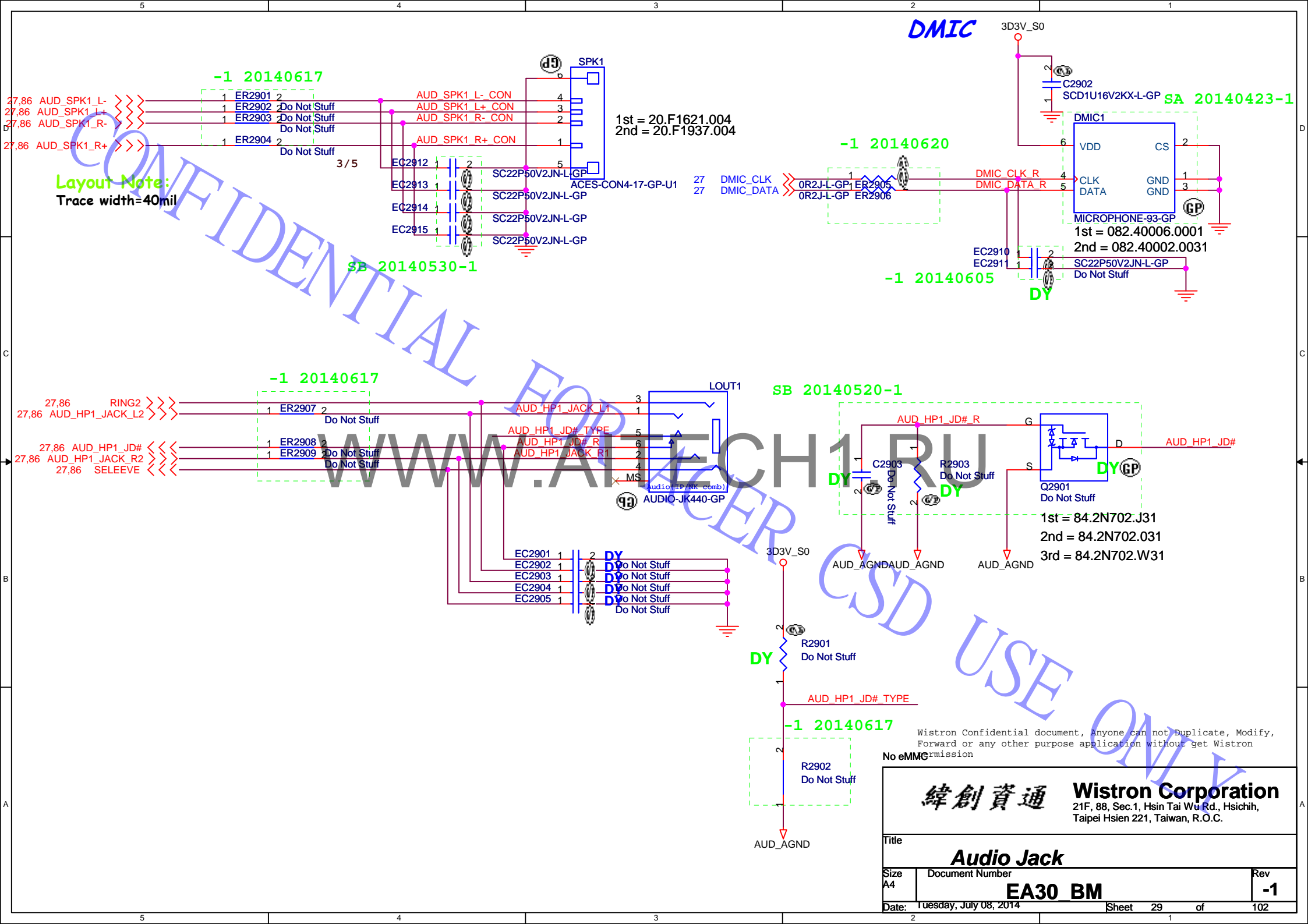


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Title		
Audio AMP 1001		
Size	Document Number	Rev
A4	EA30 BM	-1
Date:	Tuesday, July 08, 2014	Sheet 28 of 102





Layout Note:  
Trace width=40mil

1st = 20.F1621.004  
2nd = 20.F1937.004

DMIC

SA 20140423-1

-1 20140620

-1 20140605

DY

SB 20140520-1

1st = 84.2N702.J31  
2nd = 84.2N702.031  
3rd = 84.2N702.W31

-1 20140617

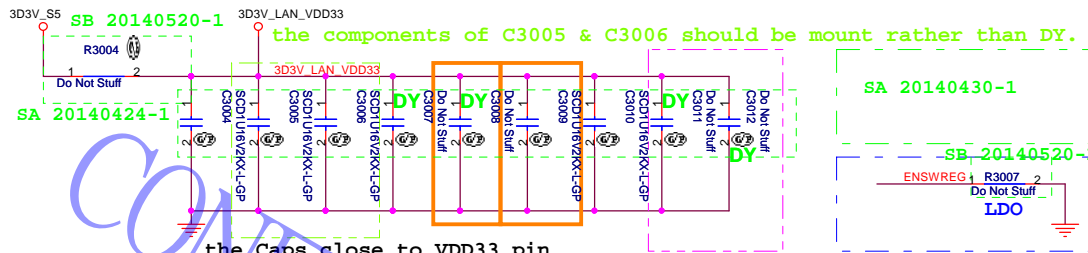
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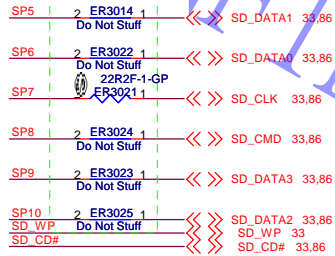
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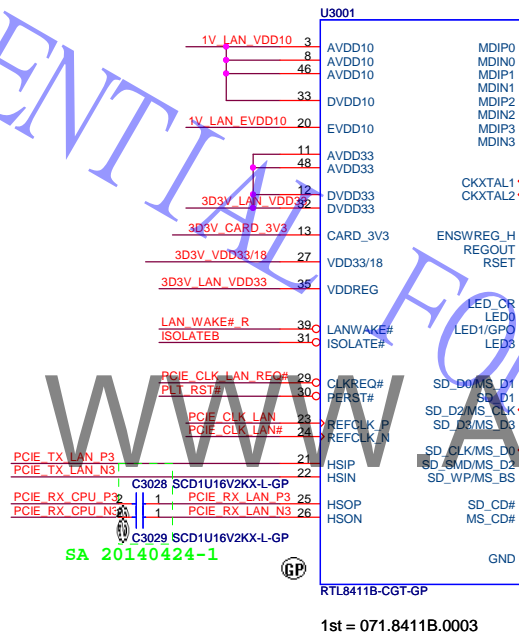
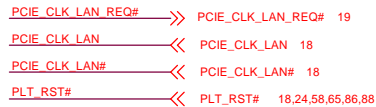
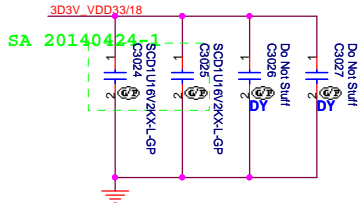
Title		
Audio Jack		
Size	Document Number	Rev
A4	EA30 BM	-1
Date	Tuesday, July 08, 2014	
Sheet	29	of 102



-1 20140618 the Caps close to VDD33 pin



SP1	SD_D7	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP2	SD_D6	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP3	SD_D5	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP4	SD_D4	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP5	SD_D3	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP6	SD_D2	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP7	SD_D1	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP8	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP9	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP10	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP11	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP12	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP13	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP14	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP15	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7
SP16	SD_D0	MS_INS#	SD_D0	MS_BS	SD_D1	MS_D2	SD_D2	MS_D3	SD_D3	MS_D4	SD_D4	MS_D5	SD_D5	MS_D6	SD_D6	MS_D7	SD_D7

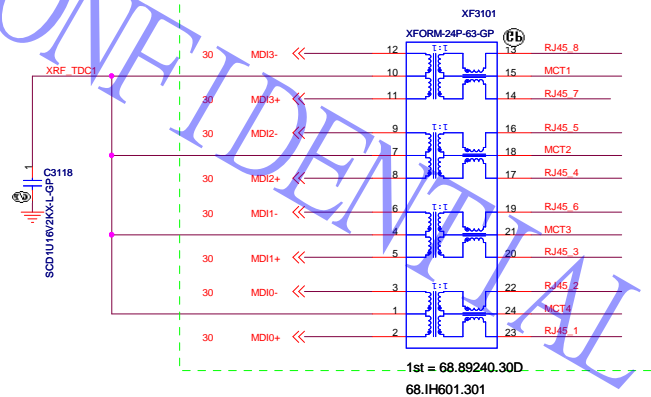


SSID = LAN

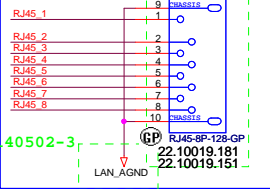
SB 20140528-1

» RJ45\_1 86  
» RJ45\_2 86  
» RJ45\_3 86  
» RJ45\_4 86  
» RJ45\_5 86  
» RJ45\_6 86  
» RJ45\_7 86  
» RJ45\_8 86

SA 2040428-1



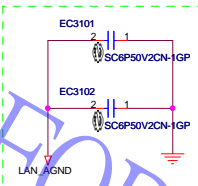
-1M 20140630



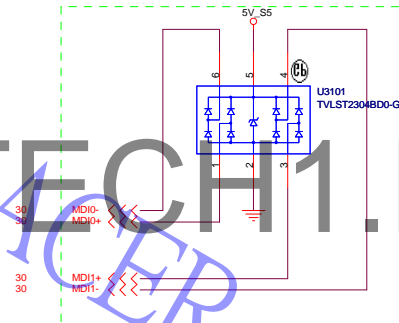
SA 20140502-3

LAN RJ45 connector

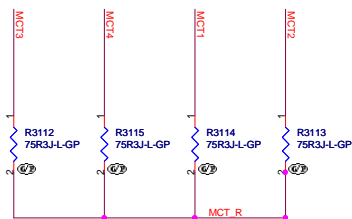
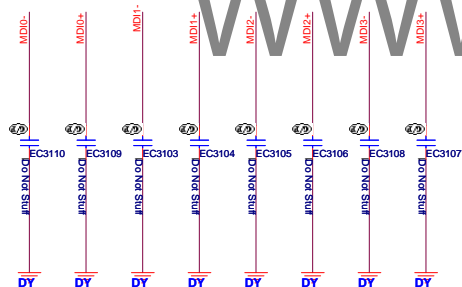
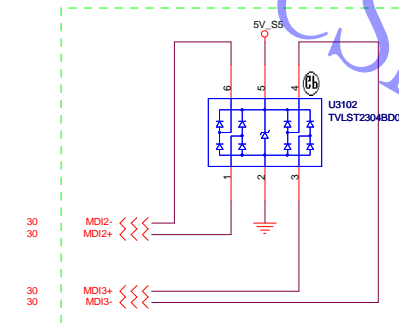
SA 20140506-2



SA 20140423-1



SA 20140423-1



SA 20140502-1

No eMMC

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Title			(LAN+VGA) CONNECTOR
Size	Document Number	Rev	
Custom	EA30 BM	-1	
Date	1/8/2014, July 06, 2014	Sheet	31 of 102

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Title			
RTS5229(CARD READER)			
Size	Document Number		Rev
A4	EA30 BM		-1
Date: Tuesday, July 08, 2014		Sheet 32	of 102

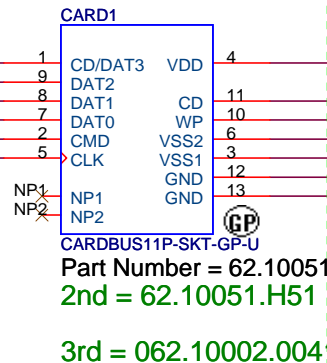
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# SD//MS Card Reader

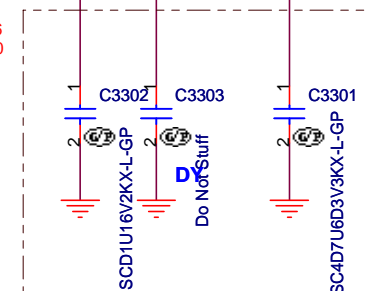
-1 20140605

SA 20140505-1

30,86 SD\_DATA3  
30,86 SD\_DATA2  
30,86 SD\_DATA1  
30,86 SD\_DATA0  
30,86 SD\_CMD  
30,86 SD\_CLK



Close to Connector



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Title

**CARD Reader CONN**

Size  
Custom

Document Number

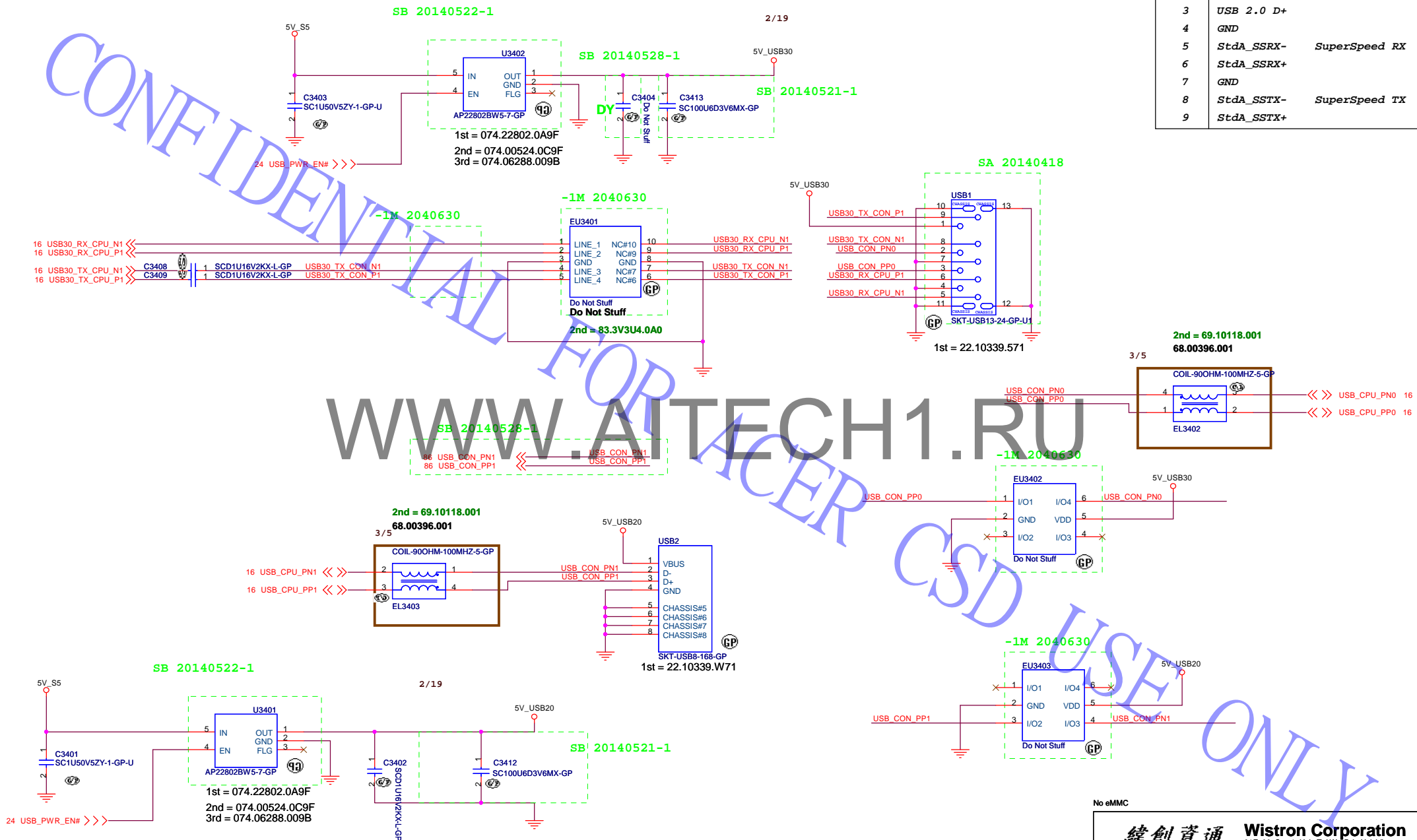
**EA30 BM**

Rev  
**-1**

Date: Tuesday, July 08, 2014

Sheet 33 of 102

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



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Title			
<b>USB 2.0/3.0 Port</b>			
Size A3	Document Number		Rev
	<b>EA30 BM</b>		<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 34 of	102

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No eMMC

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB CHARGER			
Size	Document Number		Rev
A3	EA30_BM		-1
Date:	Tuesday, July 08, 2014		Sheet 35 of 102

### *DDR3 DRAM PWROK*

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		ms	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

**COREPWROK**

*From EC* <sup>SB 20140520-1</sup>  
-----

24 SYS\_PWROK  
Delay 104ms with ALL\_SYS\_PWRGO

13/8/22

*To EC*

## ***ANNIE Run Power***

13/9/18

2013/04/09

### *Discharge circuit*

2013/07/14

SA 20140423-1

303V

1 R2618 2

Do Not Stuff

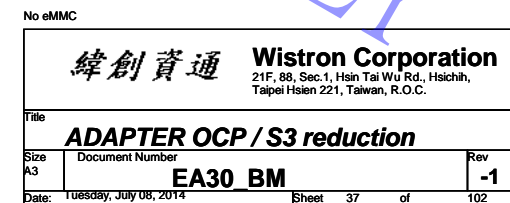
DY

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Title			
<b>Power Plane Enable &amp; SEQUENCE</b>			
Size A2	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
Date: Tuesday, July 08, 2014		Sheet 36	of 102



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Title			
DS3			
Size	Document Number		Rev
A4	EA30 BM		-1
Date: Tuesday, July 08, 2014		Sheet 38 of	102

Power Sequence

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Title			
1D05 M			
Size	Document Number	Rev	
Custom	EA30 BM	-1	
Date:	Tuesday, July 08, 2014	Sheet	39 of 102

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Title			
Connected Standby1			
Size	Document Number		Rev
A	EA30 BM		-1
Date:	Tuesday, July 08, 2014		Sheet 40 of 102

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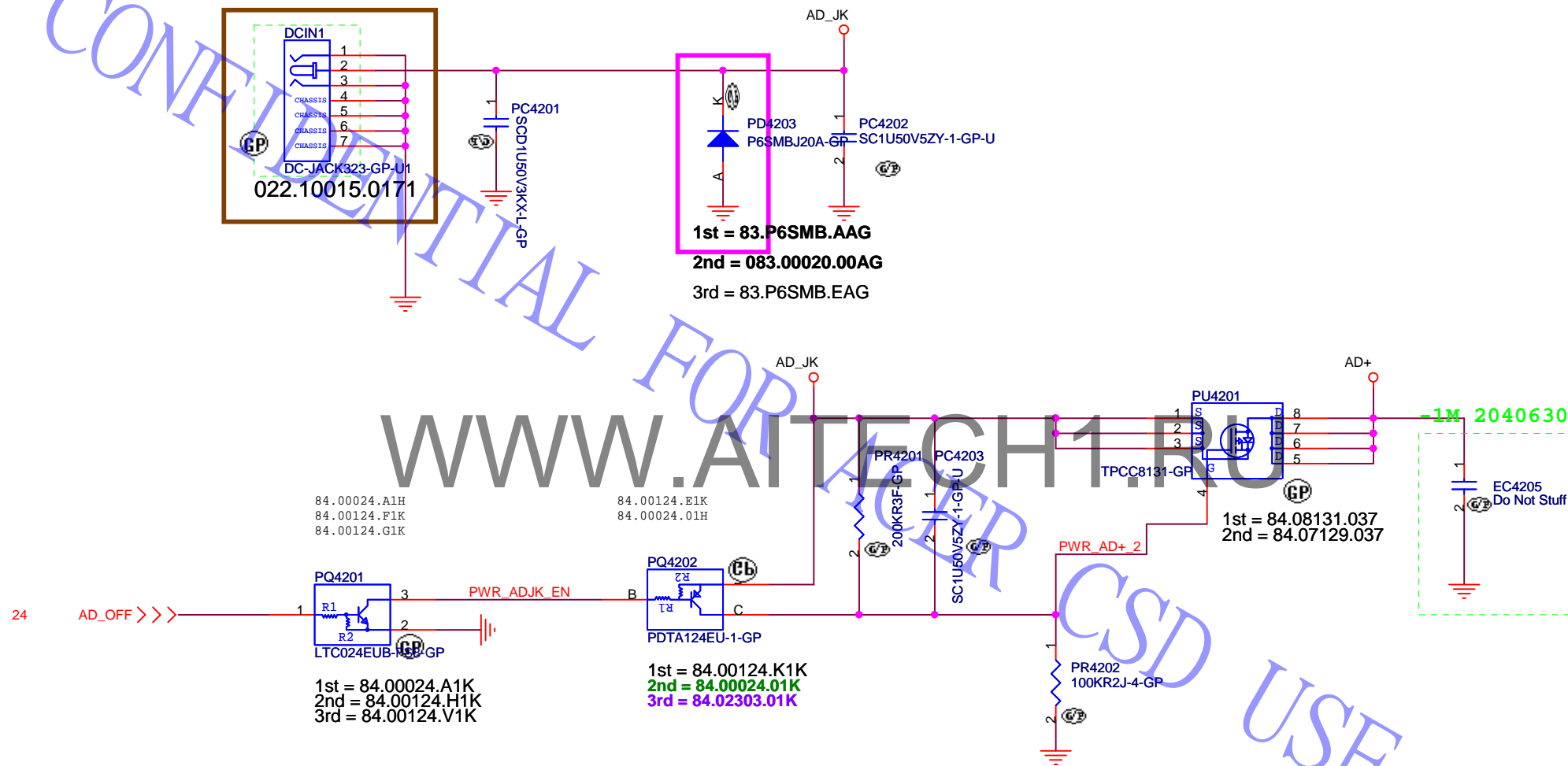
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Title			
Connected Standby2			
Size	Document Number		Rev
A	EA30 BM		-1
Date:	Tuesday, July 08, 2014		Sheet 41 of 102

## Adaptor in to generate DCBATOUT



vic0103

--

DC IN connector

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Title

***DCIN JACK***

Size  
A4

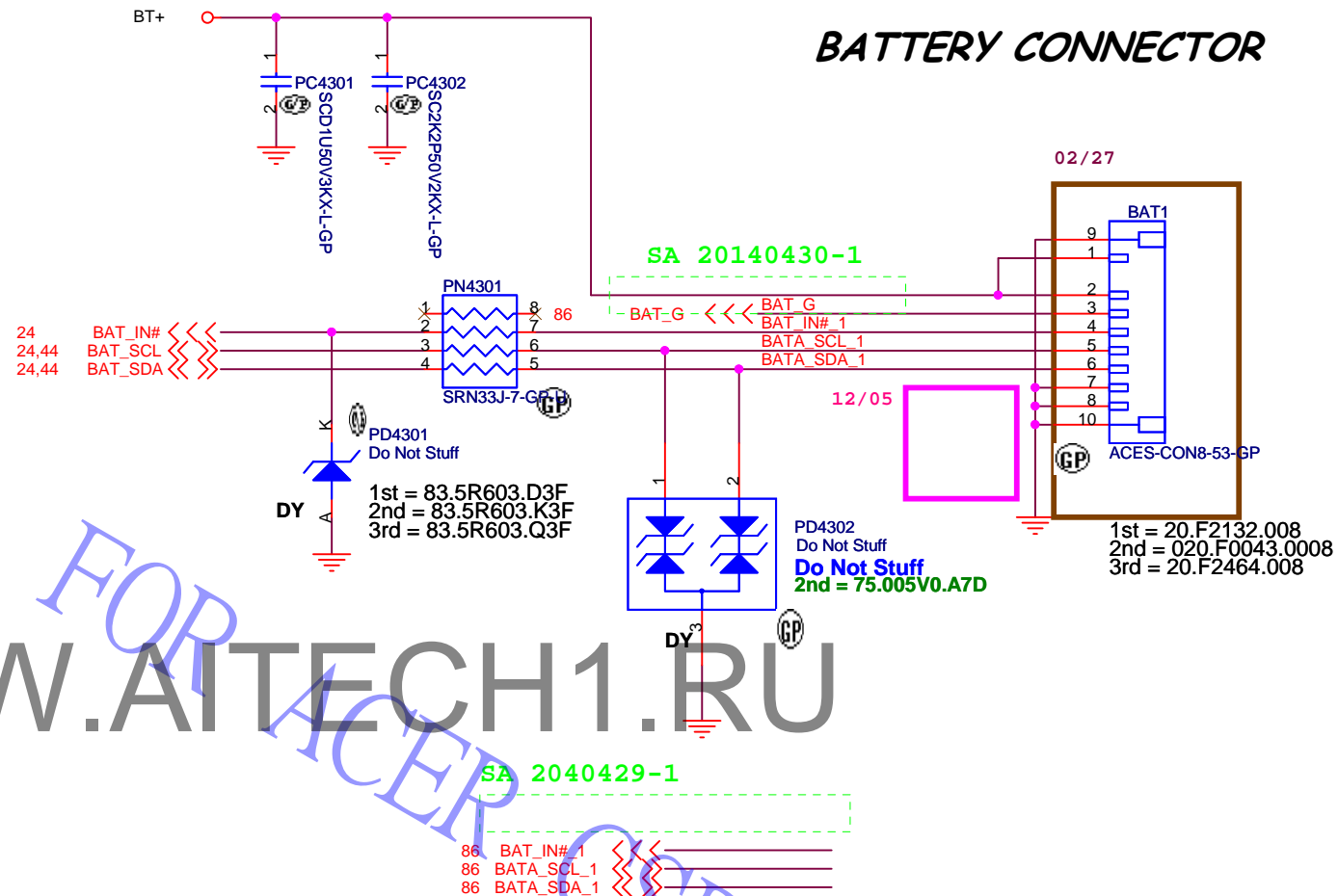
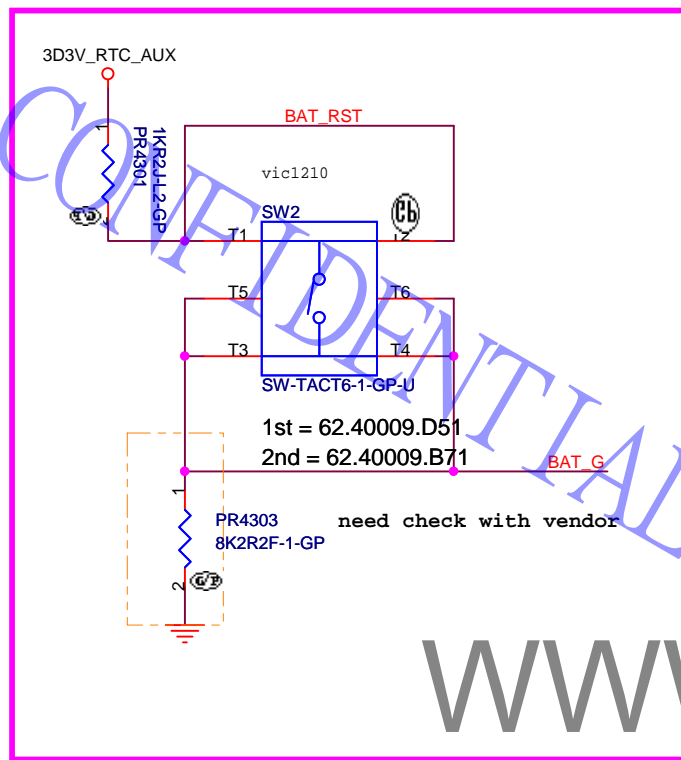
Document Number

**EA30 BM**

Rev	
-----	--

Date: Tuesday, July 08, 2014

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Title

**BATT CONN**

Size  
A4

Document Number

**EA30 BM**

Rev

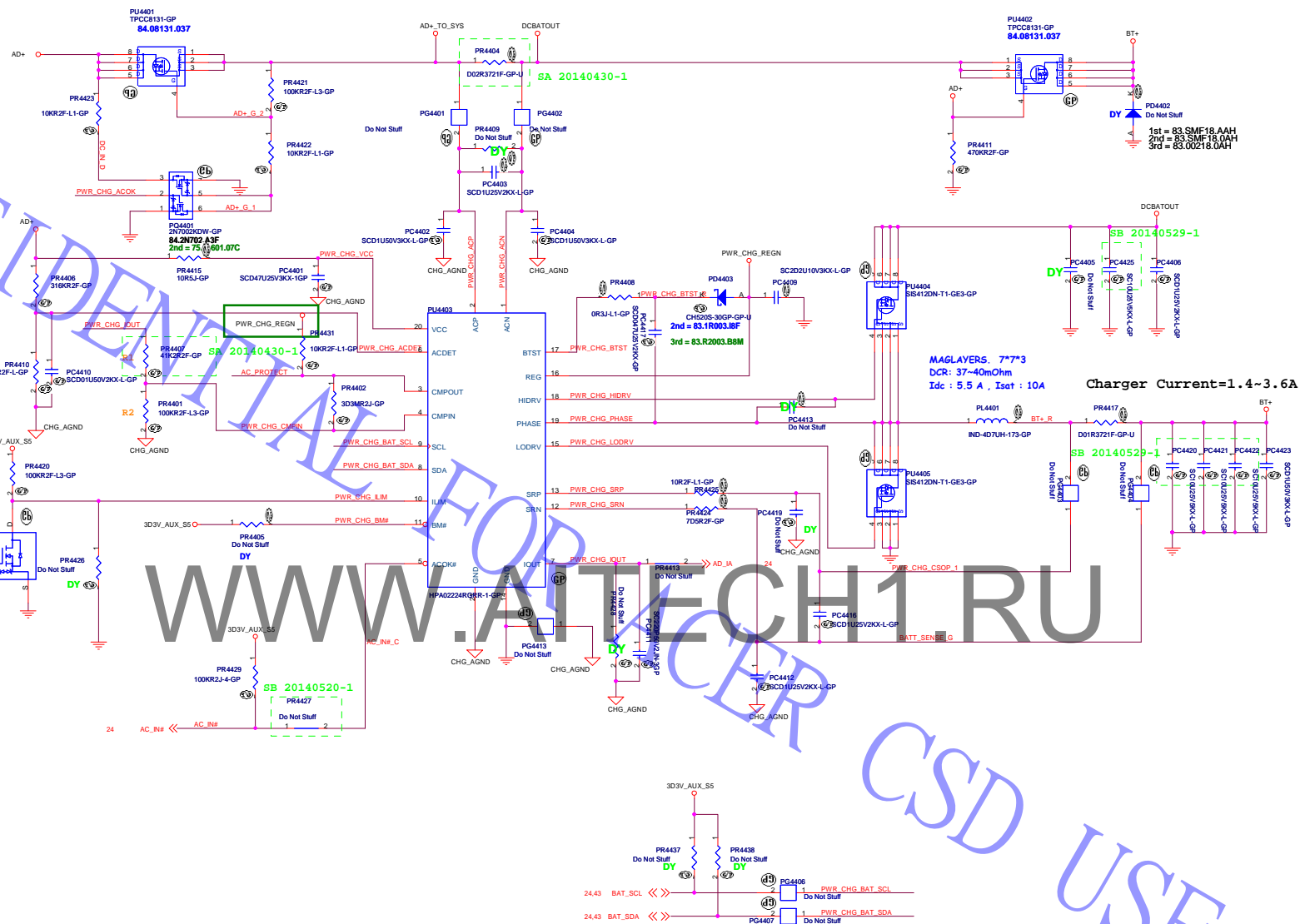
**-1**

Date: Tuesday, July 08, 2014

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SSID = Charger

AD+ total power	R1	R2
40W	41.2K	100K



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Title			
<b>CHARGER_BQ24727</b>			
Size	Document Number	Rev	
A2	<b>EA51 BM</b>	<b>-1</b>	
Date:	Tuesday, July 08, 2014	Sheet 44	of 102

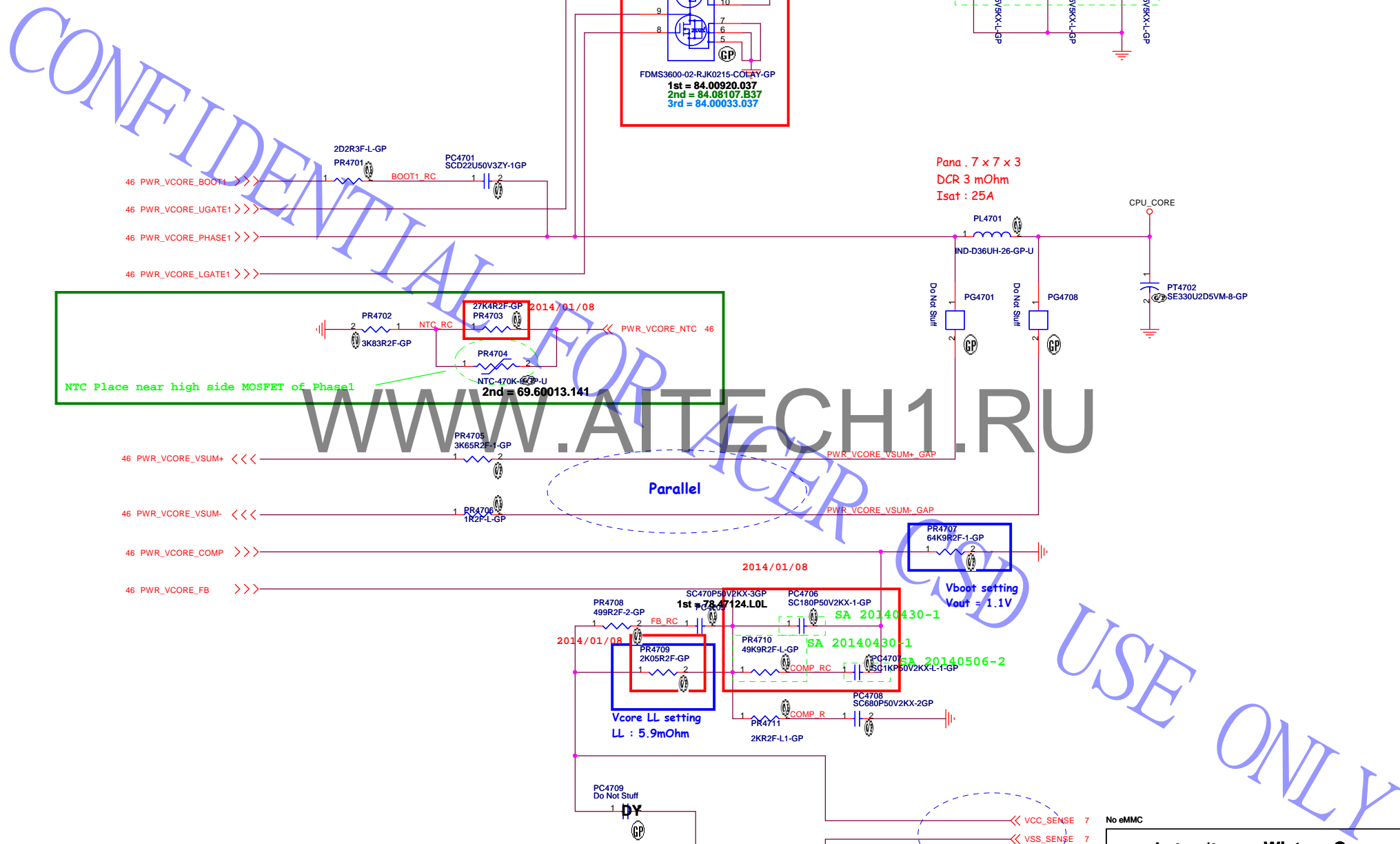




Title			
TPS51225 5V/3D3V			
Size A2	Document Number		Rev
	EA51_BM		-1
Date:	Tuesday, July 08, 2014	Sheet 45 of	102

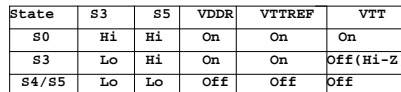
No eMMC

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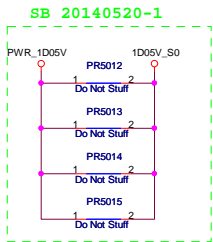
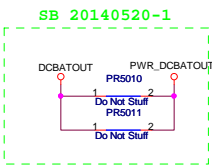
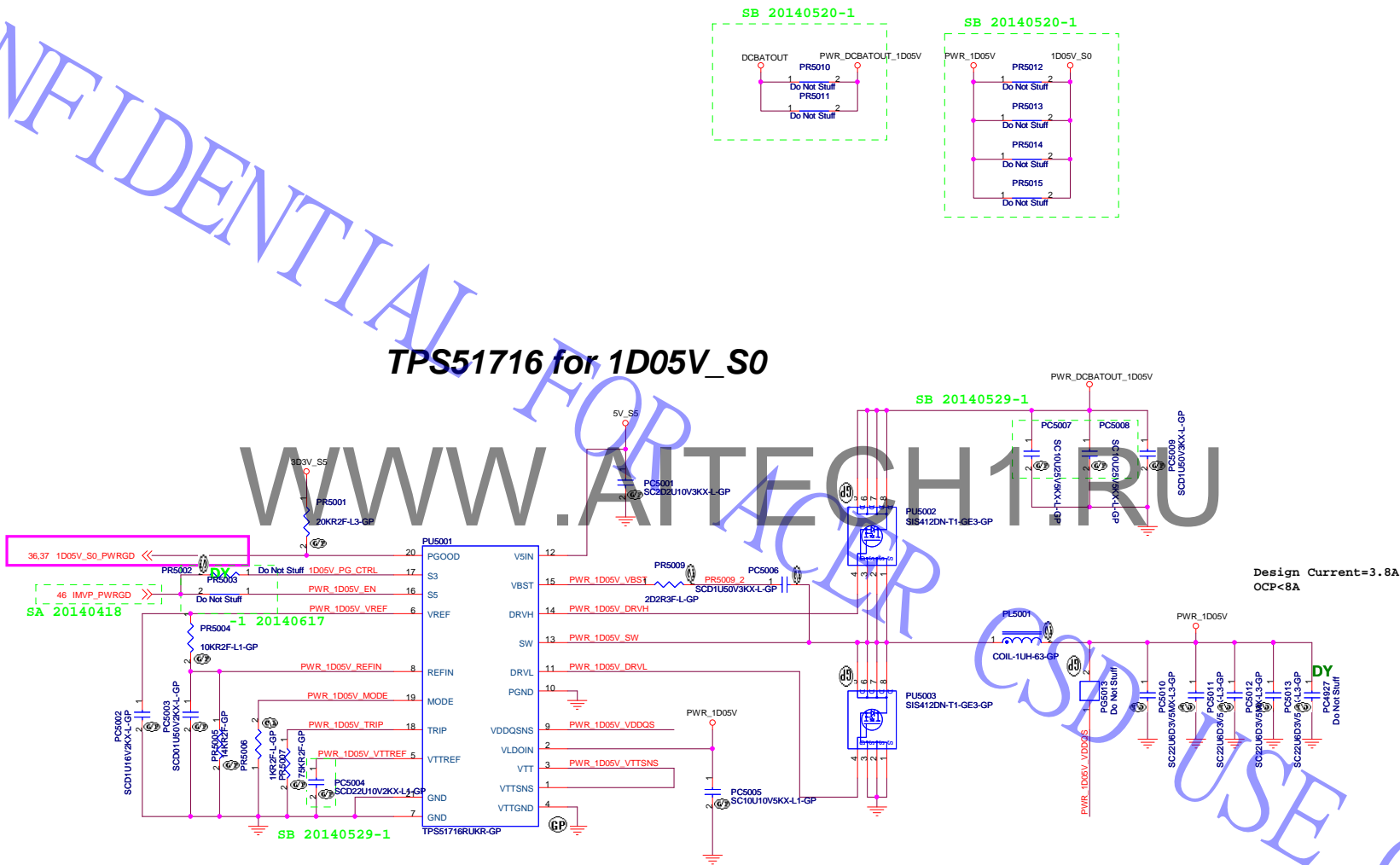
## RT8231 for VDDQ



SSID = PWR.Plane.Regulator\_1p05v

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TPS51716 for 1D05V\_S0



36.37 1D05V\_S0\_PWRGD <<

46 1MVP\_PWRGD >>  
SA 20140418

-1 20140617

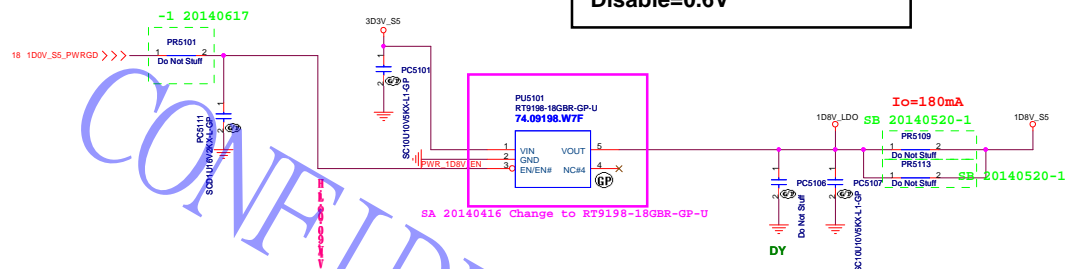
SB 20140529-1

Design Current=3.8A  
OCP<8A

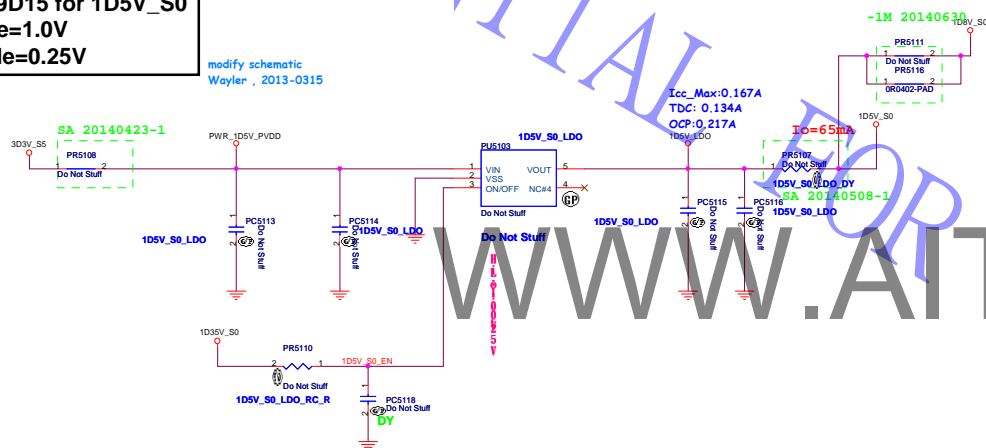
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-2)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

TLV70218DBVR for 1D8V\_S5  
Enable=0.9V  
Disable=0.6V



modify schematic  
Wayler , 2013-0315



SA 20140418

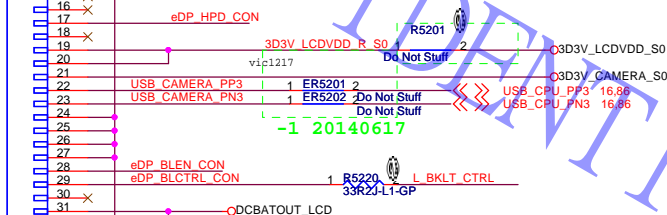
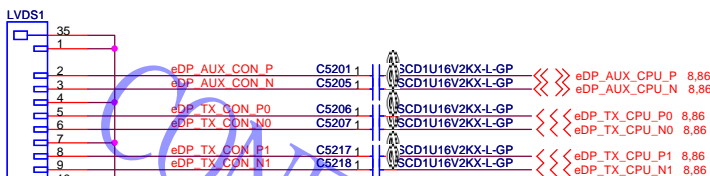
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Title			
<b>LDO 1D8V&amp;1D5V(SYW232)</b>			
Size A2	Document Number		Rev
	<b>EA51_BM</b>		<b>-1</b>
Date:	Tuesday, July 08, 2014	Sheet 51 of	102

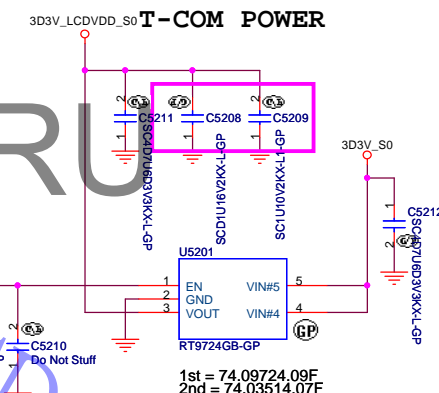
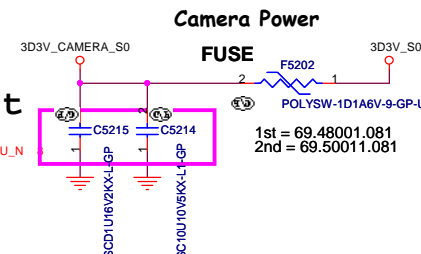
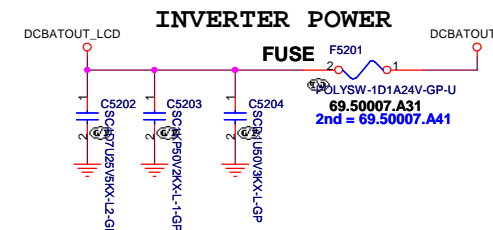
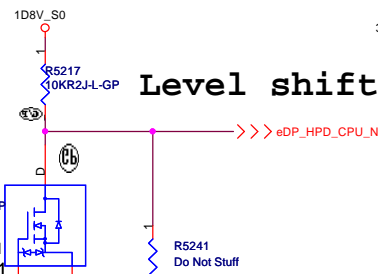
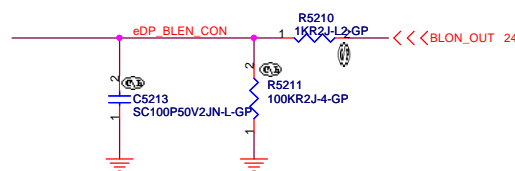
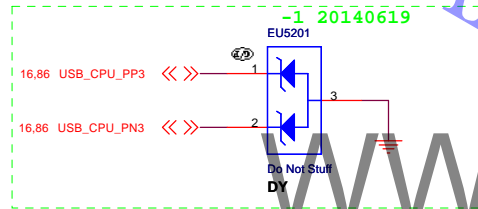
SSID = VIDEO

vic1210

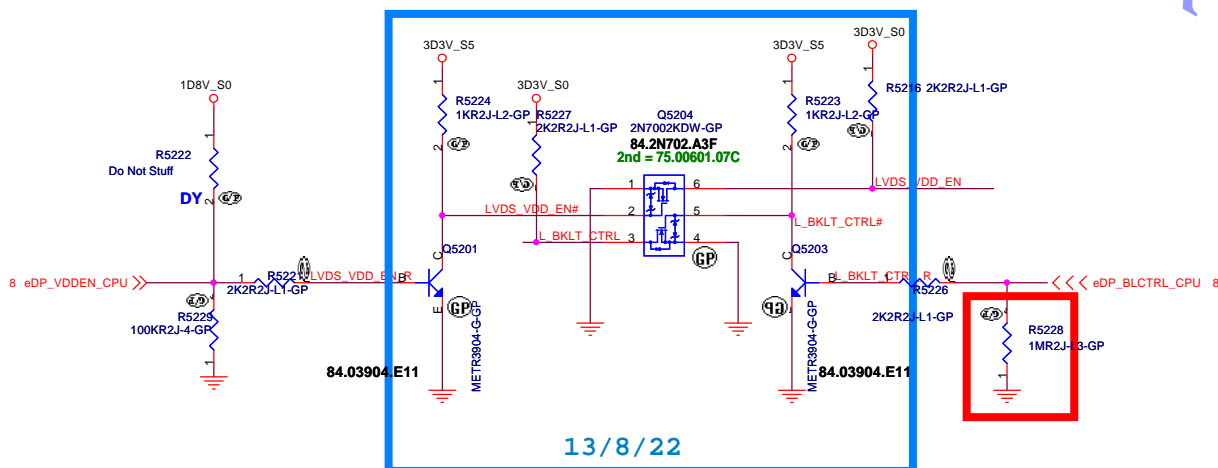
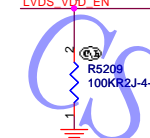


STAR-CON-1-GP-U1  
1st = 20.K0809.034  
2nd = 20.K0678.034

EDP connector



Layout 40 mil



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Title			
EDP Connector			
Size A3	Document Number	Rev	
	EA30 BM	-1	
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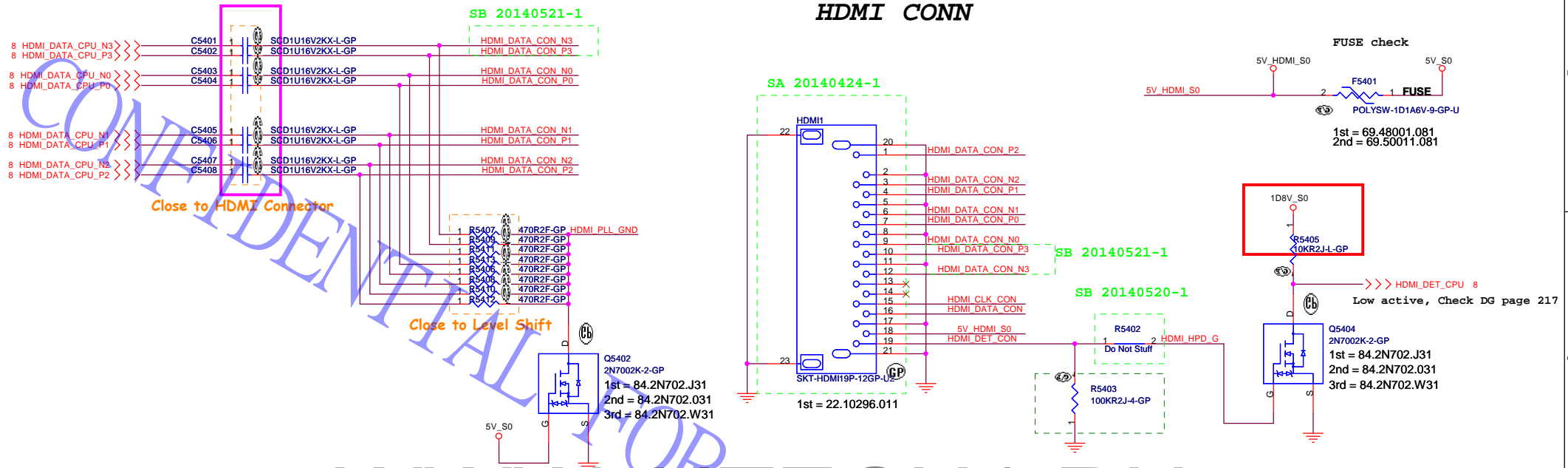
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No eMMC

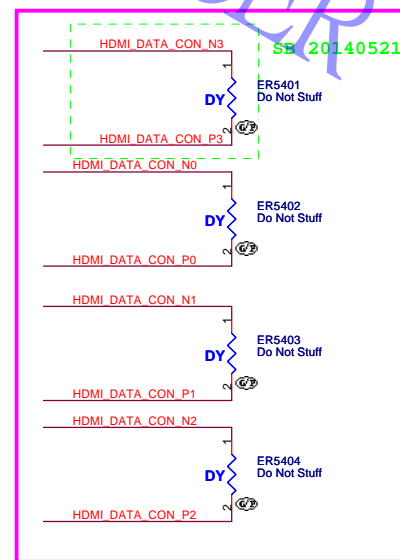
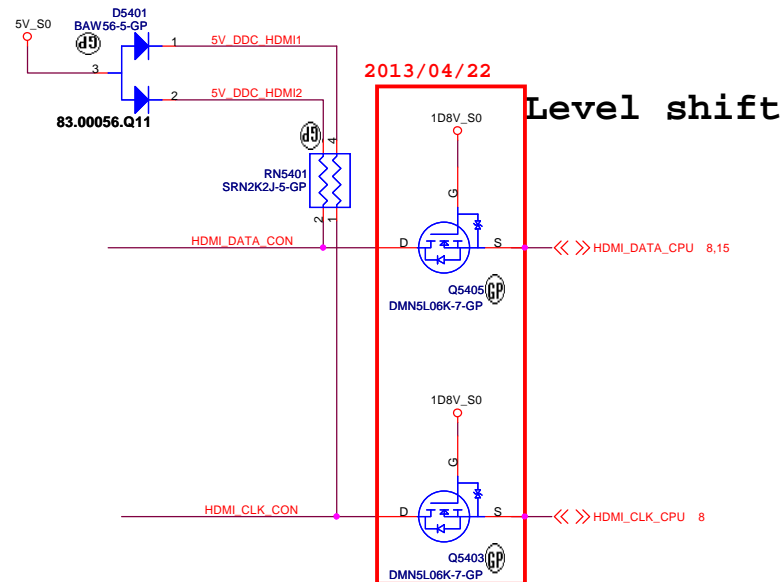
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Title			
CRT Board Connector			
Size	Document Number		Rev
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SSID = VIDEO

# HDMI Level Shifter & CONNECTOR



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Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3	EA30 BM	-1
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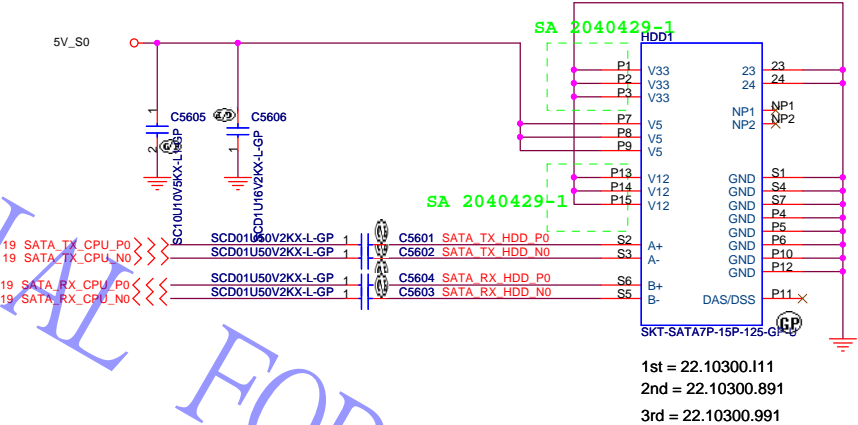
No eMMC

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Title			
Display Port			
Size	Document Number		Rev
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SSID = SATA

SATA HDD Connector

SSID = SATA



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AC coupling caps near connector<100 mils

No eMMC



**SSID = Wireless** *Mini Card Connector(802.11a/b/g/n)*

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### MINICARD(WLAN)

Document Number
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EA30\_BM

	-1
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Date: Tuesday, July 08, 2014

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SSID = Wireless

Mini Card Connector(mSATA)

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Title			
WWAN CONN			
Size	Document Number		Rev
A4	EA30 BM		-1
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SSID = mSATA

Mini Card Connector(mSATA)

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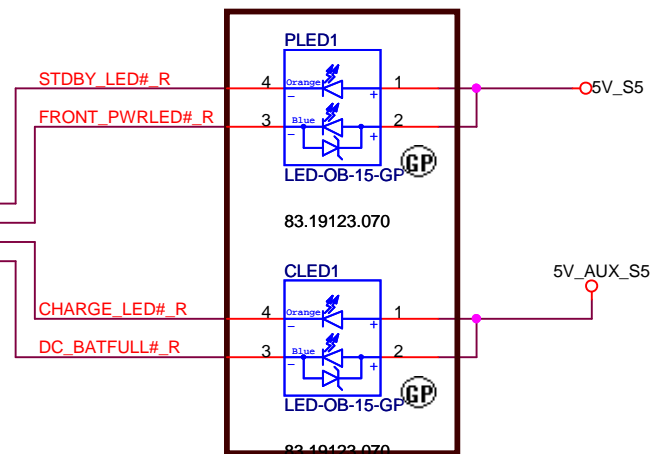
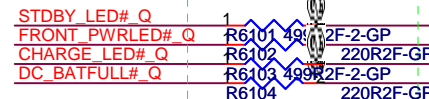
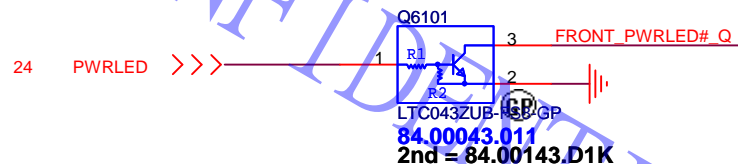
No eMMC

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
mSATA Connector			
Size	Document Number		Rev
A4	EA30 BM		-1
Date: Tuesday, July 08, 2014		Sheet 60	of 102

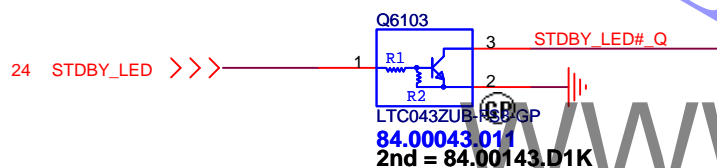


SSID = User.Interface

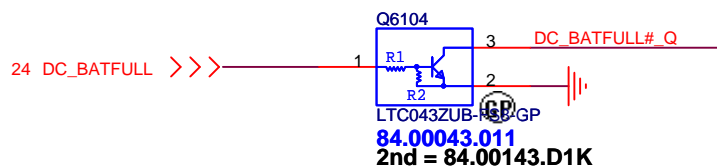
## Power button\_LED



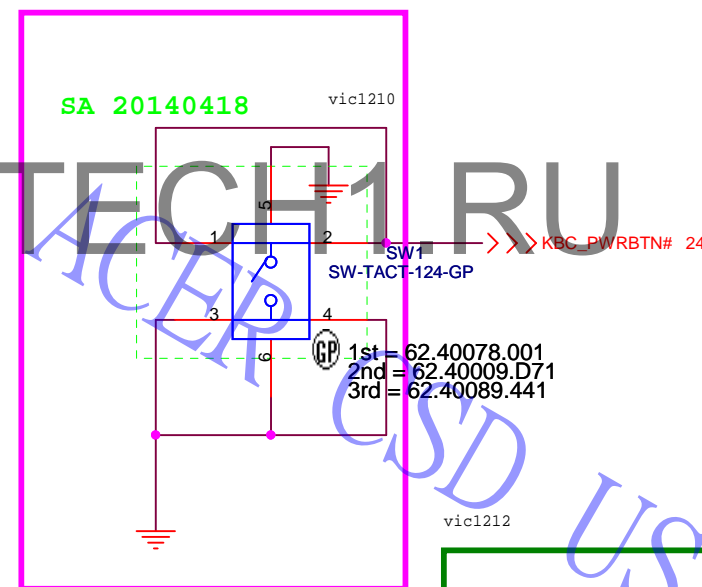
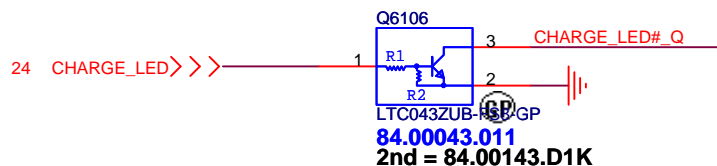
## Power STDBY\_LED



## Battery LED2 (DC\_BATFULL)



## Battery LED1 (CHARGE)



No eMMC

緯創資通

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Title

LED Bard/Power Button

Size  
A4

Document Number

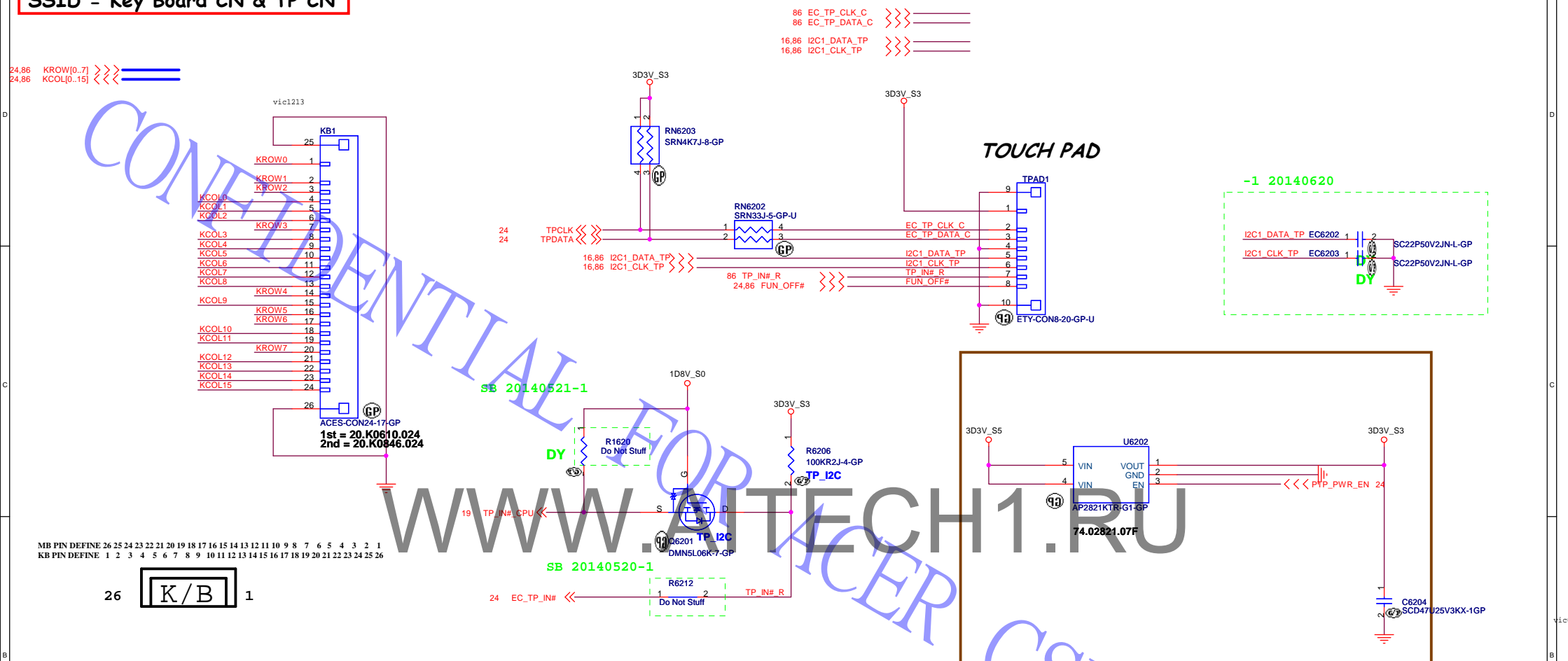
EA30 BM

Rev  
-1

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**SSID = Key Board CN & TP CN**



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Title \_\_\_\_\_

<b>Key Board/Touch Pad</b>
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Size	Document Number	Rev
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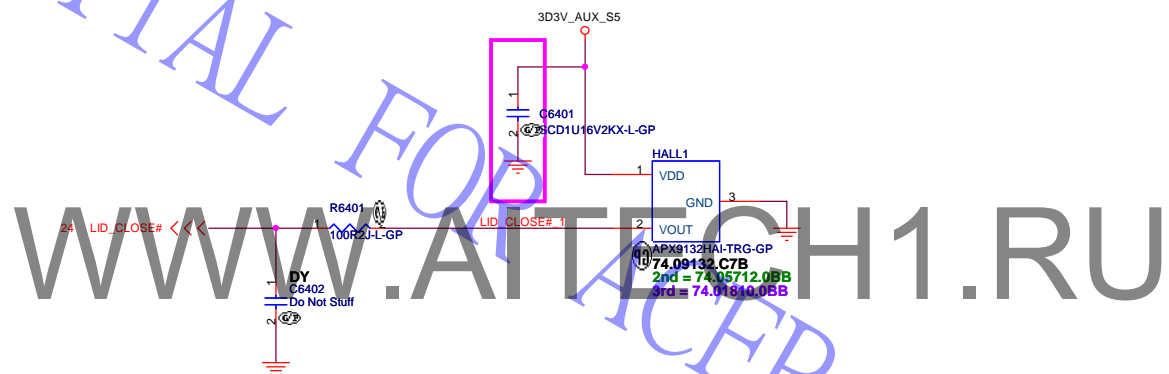
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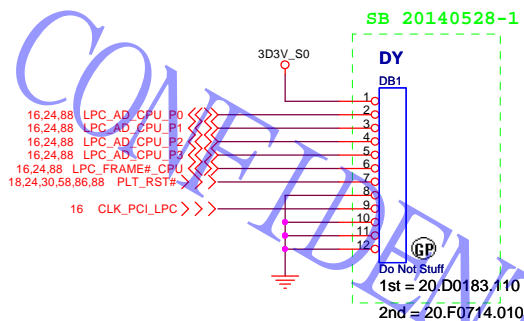
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Title			
IO Board Connector			
Size	Document Number		Rev
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Title			Dubug connector	
Size	Document Number		Rev	
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(Blanking)

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Title <b>SENSOR HUB</b>			
Size A3	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
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# Free Fall Sensor

## Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"  
\*SDO="L"; address="38h"

\*CS="H"; mode="I2C"  
CS="L"; mode="SPI"

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Title

**G Sensor**

Size  
A

Document Number

**EA30 BM**

Rev

**-1**

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Title			
Thunderbolt (1/5)			
Size	Document Number	Rev	
Custom	EA30 BM	-1	
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Title		
Thunderbolt (2/5)		
Size	Document Number	Rev
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Title Thunderbolt (3/5)	
Size Custom	Document Number EA30 BM
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Title			
Thunderbolt (4/5)			
Size	Document Number	Rev	
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Title			
Thunderbolt (5/5)			
Size	Document Number		Rev
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Title GPU(PEG)			
Size	Document Number	Rev	
Custom	EA30 BM	-1	
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Title			
GPU (DIGITALOUT)			
Size	Document Number		Rev
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GPU-VRAM1,2 (1/4)			
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GPU-VRAM3,4 (2/4)			
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GPU-VRAM5,6 (3/4)			
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GPU-VRAM7,8 (4/4)			
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RT8812A VGA CORE			
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Title			
Switchable GFX LCD(1/2)			
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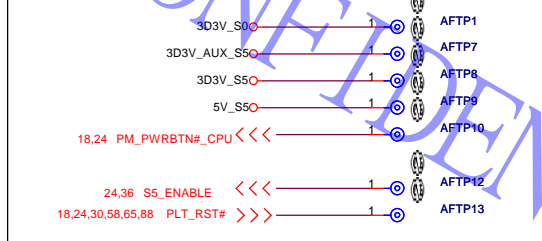
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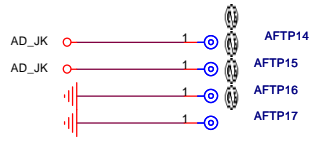
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Title			
Switchable GFX LCD(2/2)			
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## Check test point

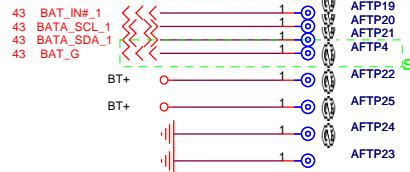
Test Point放在 Bottom side 可量測處



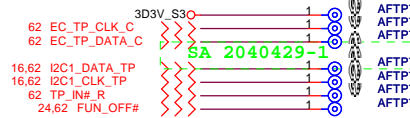
## DCIN



## BARRETY



## Touch PAD



## Speaker

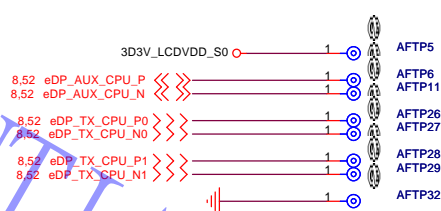


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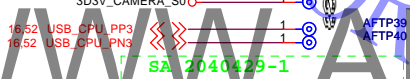
SA 2040429-1

SB 20140528-1

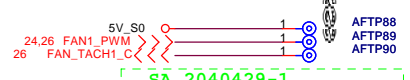
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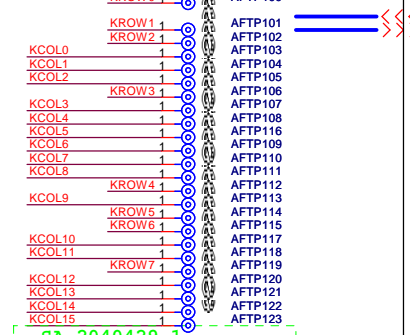
## CCD



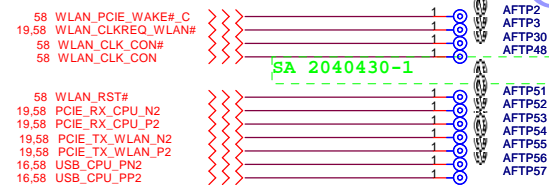
## FAN



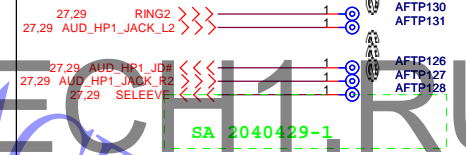
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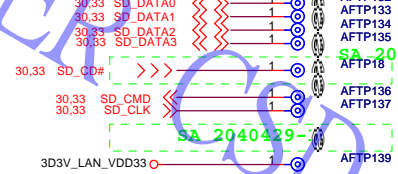
## WLAN



## Audio Jack

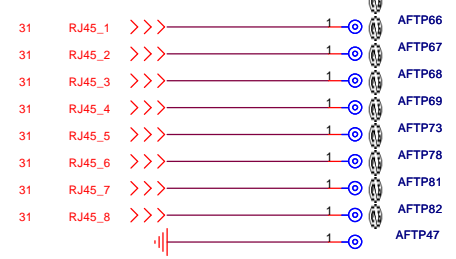


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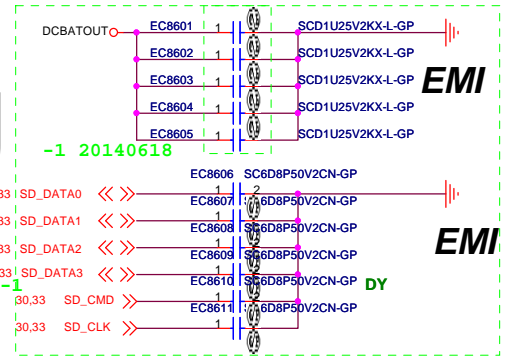


SB 20140528-1

## LAN\_RJ45 connector

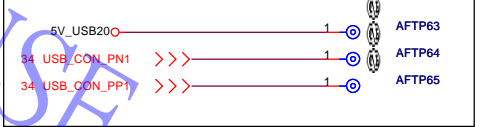


SA 20140502-3



## USB2

SB 20140528-1



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A	EA30 BM		-1
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Title			
<b>Smart Card socket</b>			
Size A	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
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Title			
Switchable GFX eDP			
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Title <b>Bottom Docking</b>			
Size A	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
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Title <b>Inter LAN WG1217LM</b>			
Size A3	Document Number <b>EA30 BM</b>		Rev <b>-1</b>
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Title		
LAN Switch		
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title			
<b>PCH_XDP</b>			
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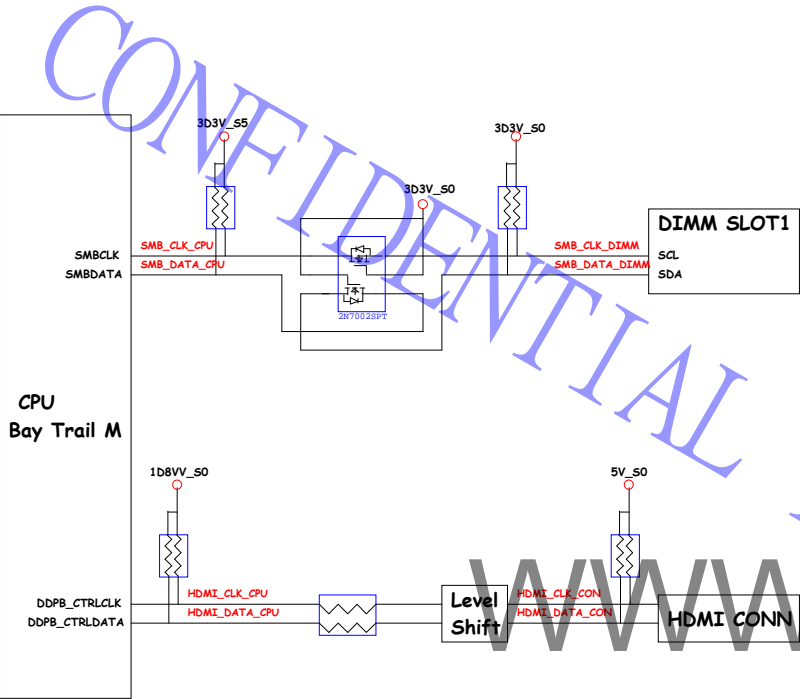
Timing diagram for the 3.3V Level showing the sequence of signals during a power-up event. The diagram includes signals for RTC\_AUX\_S5, RTC\_RST#, 3D3V\_AUX5V\_AUX, ECRST#, 3V\_5V\_EN, 5V\_S5/3D3V\_S5, 1DOV\_S5, 1DOV\_S5\_PWRGD, 1D5V\_S5, 1D5V\_S5\_FG, 1D2V\_S5, 1D2V\_S5\_PWRGD, RSMRST#\_KBC, PM\_SLP\_S4#, DDR3\_DRAM\_PWRCK, 1D35V\_S3, PM\_SLP\_S3#, VCC\_CORE & GFX\_CORE, IMVP\_PWRGD, 1DOV\_S0, 1DOV\_S0\_FG, 1D05V\_S0, 1D05V\_S0\_PG (ALL\_SYS\_PWRGD to EC), 1D35V\_S0 & 1D35V\_CRT\_S0, 1D5V\_S0, 1D5V\_S0\_FG, 3D3V\_S0 & 5V\_S0, 0d675V\_S0, SYS\_PWRCK (Base on ALL\_SYS\_PWRGD to delay 110ms), COREPWRCK, 1.35V Level, DDR3\_VCCA\_PWRGD, and FLT\_RST#. A red arrow indicates a delay of  $T1 = 10 \mu s$  between RSMRST#\_KBC and PM\_SLP\_S4#. A red arrow indicates a delay of  $T1 = 110 ms$  between SYS\_PWRCK and COREPWRCK. A red arrow indicates a delay of  $T1 = 110 ms$  between 1.35V Level and FLT\_RST#.

[illegible]

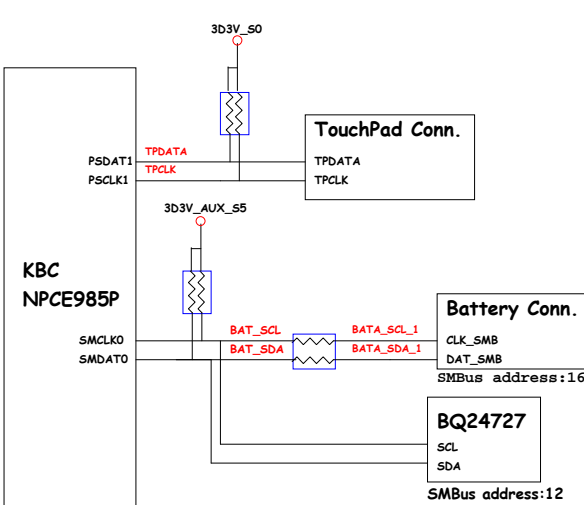




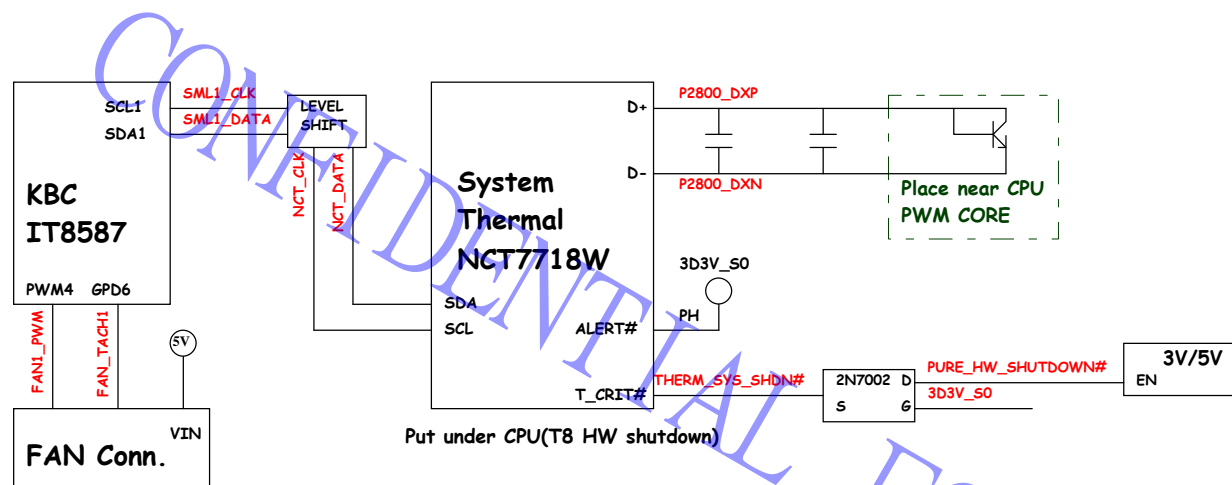
PCH SMBus Block Diagram



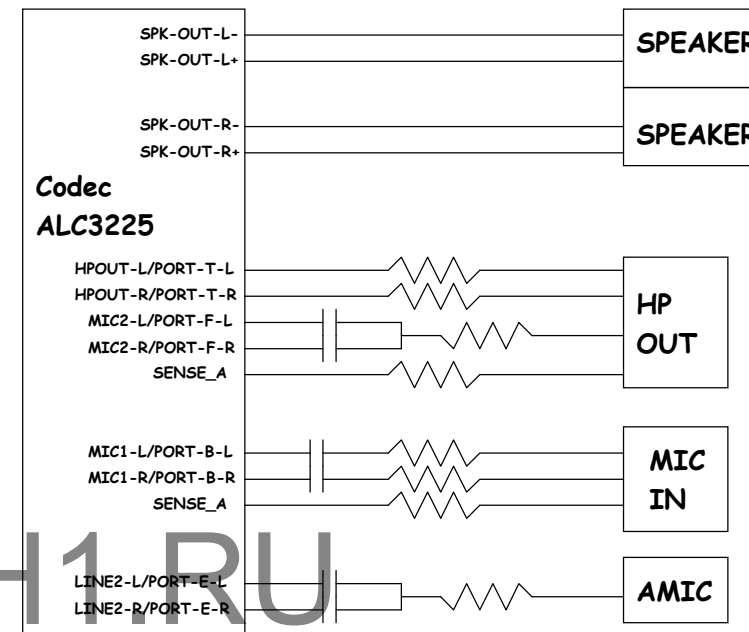
KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



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